INSTRUCTION MANUAL

MODEL 189
4 MHz SWEEP/ FUNCTION GENERATOR

WAVETEK
SAN DIEGO

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

INSTRUCTION MANUAL

MODEL 189
4 MHz SWEEP/ FUNCTION GENERATOR

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do no bypass earth grounding with two wire extension cords, plug adapters, etc.

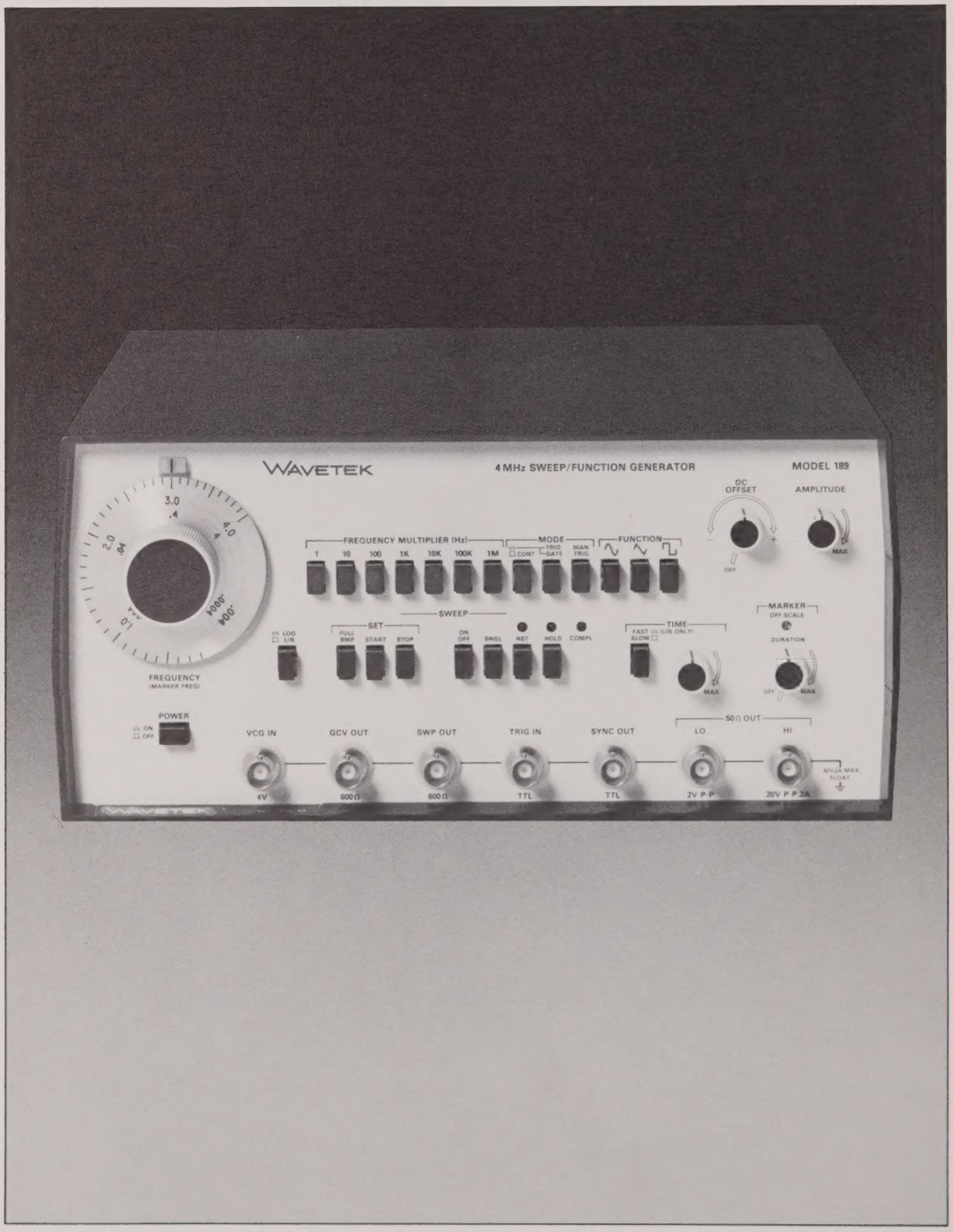
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptical is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.



Model 189 4MHz Sweep/Function Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 189

The Wavetek Model 189, 4 MHz Sweep/Function Generator, is a precision source of sine, triangle and square waveforms plus dc voltage. All waveforms are front panel variable from .4 mHz to 4 MHz and can be internally or externally modulated. Frequencies are variable linearly or logarithmically within a frequency range. When used as a sweep generator, an internal ramp generator provides a recurring or non-recurring sweep over a 1000:1 (linear) frequency range or 10,000:1 (logarithmic) frequency range. A frequency marker is included that stops the sweep ramp to give a bright (increase dwell time) indicator at the selected frequency. Output can be continuous or the generator can be triggered or gated by an external signal or a front panel switch. Amplitude of the waveforms is variable form 10V peak-to-peak into 50Ω down to 30 mV peak-to-peak. DC reference of the waveform can be offset positively or negatively.

The two selectable waveform outputs are a 20V peak-to-peak maximum and a 2V peak-to-peak maximum (20 dB down from 20 Vp-p); both may be varied over a 30 dB range. Auxiliary outputs are a TTL level sync, a 600Ω sweep ramp (this signal also carries the frequency marker) and a 600Ω generator control voltage signal whose level is proportional to the main generator frequency.

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms
Sine ∿ , triangle ∿ , square ⊓ , and dc.

Operational Modes
Continuous: Generator runs continuously.

Triggered: Generators one complete waveform cycle at selected frequency when triggered.

Gated: As triggered mode, except output continues for duration of gate signal. Last cycle started is completed.

Sweep: Recurring low-to-high or high-to-low frequency change. Range, rate and mode (linear or logarithmic) selectable.

Single Sweep: One sweep and holds at stop frequency.

Frequency Range
0.004 Hz linear (0.0004 Hz log) to 4 MHz in 7 overlapping decade ranges:

×1	0.004 (0.0004) to 4 Hz
×10	0.04 (0.004) to 40 Hz
×100	0.4 (0.04) to 400 Hz
×1K	4 (0.4) Hz to 4 kHz
×10K	40 (4) Hz to 40 kHz
×100K	400 (40) Hz to 400 kHz
×1M	4 (0.4)kHz to 4 MHz

Function Output
∿ , ∿ , ⊓ selectable and variable to 20 Vp-p (10 Vp-p into 50Ω) HI output, and to 2 Vp-p (1 Vp-p into 50Ω) LO output. Both outputs varied with a 30 dB vernier. Peak output current is 100 mA maximum (HI output) into 50Ω (200 mA peak into a short circuit). Source impedance is 50Ω.

DC Offset and DC Output
Waveform offset and dc output selectable and variable through HI and LO BNC outputs. DC output selectable by not selecting a waveform function. HI output is ±10V max (±5V into 50Ω) as offset or Vdc output. Signal-peak plus offset limited to ±10V (±5V into 50Ω). LO output is ±1V max (±0.5V into 50Ω) as is signal-peak plus offset limit. DC offset plus waveform attenuated proportionately at LO output.

Sweep Control
Full Sweep: Sweep start/stop points set for full width of range and mode (lin/log) selected.

Lin/Log: Linear or logarithmic sweep.

Set Start and Set Stop: Sets sweep end points to frequency dial setting and stores selected frequencies in digital memory.

Hold: Sweep stops at instant of hold command activation.

Fast/Slow: 100 μs to 600 ms range (linear sweep only) and 20 ms to 120s range.

Sweep Time: Selects sweep duration within fast or slow range.

Marker: Zero slope in a portion of the 0 to 4V sweep out ramp signal. Occurs when instantaneous output frequency equals frequency dial setting and for selectable duration. Ramp used as X-axis scope drive; momentary zero slope stops electron beam sweep for frequency marker. Zero slope duration determines brightness.

Marker Duration: 2% to 60% of sweep time.

Sweep Annunciators
Reset: Lights when sweep is at start frequency.

Complete: Lights when sweep is at stop frequency.

Hold: Lights when sweep is held.

Marker off scale: Lights when marker (dial) is not set between start and stop frequencies. Status is updated during or at end of each sweep.

Inputs
Ext Sweep Reset: Low causes instantaneous return to start frequency. Sweep starts when high. TTL or switch closure.

Ext Sweep Hold: Low holds sweep at instantaneous frequency. Sweep resumes when high. TTL or switch closure.

VCG In: Up to 1000:1 frequency change (linear mode) or up to 10,000:1 a change (logarithmic mode) with external 0 to ±4V signal. Upper and lower frequencies limited to maximum and minimum of selected range.

Slew Rate: 2% of range per μs (linear); 0 to 100% of range in 20 ms (logarithmic).

Linearity: ±0.5% through 100K range; ±2% on 1M range.

Input Impedance: 2 kΩ.

Trigger In (TTL): Triggers and gates generator output.

Pulse Width: 50 ns minimum.

Repetition Rate: 4 MHz max.

Outputs

Sweep Out: 0 to 4V open circuit ramp. Momentary zero slope for duration of marker. Output in all modes. 600Ω source impedance.

GCV Out: 0 to 4V open circuit voltage level proportional to main generator frequency. 600Ω source impedance.

Pen Lift Out (TTL): Momentary high (or low if desired) when sweep is stopped and during reset. Not affected during marker duration.

Marker Out (TTL): High for duration of marker. When sweep is off, high at start of sweep out signal.

Sync Out (TTL): 50% duty cycle pulse at generator frequency. Drive up to 20 TTL loads.

1.2.2 Frequency Precision

Dial Accuracy
±5% of full scale.

Time Symmetry
Square wave variation from 0.2 to 4.0 on dial less than:
±1% to 100 kHz;
±5% to 4 MHz.

Drift in Hold Mode
0.25%/min. of f.s. in SLOW sweep; ±0.25%/s of f.s. in FAST.

1.2.3 Amplitude Precision

Sine variation with frequency less than: ±0.2 dB on all ranges through ×100K, referenced to 1 kHz; ±1.0 dB to 4 MHz.

1.2.4 Waveform Characteristics

Sine Distortion
Less than: 0.5% on 1K and 10K ranges; 1% on 1, 10, 100 and 100K ranges.
All harmonics 25 dB below fundamental on 1M range.

Triangle Linearity
Greater than 99% to 200 kHz.

Square Wave Rise and Fall Time
At HI output, less than 50 ns for 10 Vp-p output into 50Ω.

1.2.5 General

Environmental
Specifications apply at 25°C ±5°C. Instrument will operate from 0°C to 50°C ambient temperatures.

Dimensions
28.6 cm (11¼ in.) wide; 13.3 cm (5¼ in.) high; 26.7 cm (10½ in.) deep.

Weight
3.6 kg (8 lb) net; 5.2 kg (11 lb) shipping.

Power
90 to 128V or 180 to 256V; 48 to 66 Hz; less than 30 watts.

NOTE

All specifications apply for dial between 0.2 and 4.0; amplitude at 10 Vp-p from HI output into 50Ω termination.

SECTION 2
INITIAL PREPARATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory for operation on a 90 to 128 Vac line supply and with a 3/8 amp slow blow fuse. Instruments configured for 180 to 256 Vac have a 3/16 amp slow blow fuse. Select the appropriate fuse and 115 or 230 switch position at the rear panel when changing power sources.

2.2.2 Signal Connections

Use 3 foot RG58U 50Ω shielded cables equipped with female BNC connectors to distribute all input and output signals.

2.3 ELECTRICAL ACCEPTANCE CHECK

This checkout procedure is a general verification of generator operation. Should a malfunction be found, refer to the warranty in the front of this manual.

A two channel oscilloscope, four 3 foot 50Ω coax cables with female BNC connectors, a coax tee connector and an additional function generator are required for this procedure.

Preset the generator front panel controls as follows:

Control	Position
Dial	2.0
MODE CONT	CONT (released)
FUNCTION	⊓
DC OFFSET	OFF (ccw)
AMPLITUDE	MAX (cw)
FREQ MULT	1K
LOG/LIN	LIN (released)
SWEEP ON/OFF	OFF (released)
SWEEP SNGL	Released
SWEEP RST	Depressed
SWEEP HOLD	Released
TIME	SLOW, 12 o'clock
MARKER	OFF (ccw)
MODE TRIG/GATE	GATE (released)

Set up the oscilloscope and Model 189 as shown in figure 2-1 and perform the steps in table 2-1.

2.4 CHANGING THE OUTPUT IMPEDANCE

The output impedance is normally:

HI 10V p-p (50Ω source) into 50Ω.
LO 1V p-p (50Ω source) into 50Ω.

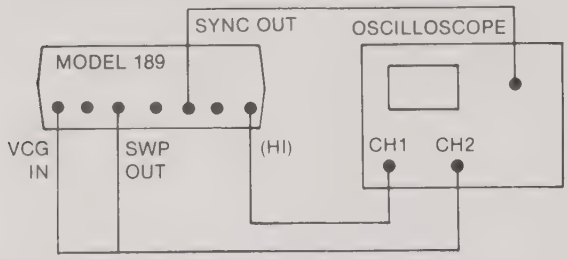


Figure 2-1. First Setup

Amplitude is normally variable over 30 dB for each output with a 50 dB amplitude range available by utilizing both outputs.

If simultaneous 600Ω and 50Ω output impedances are desired:

1. Change value of R148 from 499Ω to 604Ω.
2. Remove R149.

The result is:

HI 10V p-p (50Ω source) into 50Ω.
LO 10V p-p (600Ω source) into 600Ω.

Amplitude is variable over 30 dB with −30 dB lowest possible amplitude. Square wave rise and fall time is less than 150 ns. Any value greater than 600Ω may also be substituted for the value of R148 for other output impedances.

To increase the range of the variable amplitude control in a modified unit beyond 30 dB, decrease the value of R124 as necessary. Waveform quality relative to the standard unit is not guaranteed below −30 dB and above 20 kHz.

Table 2-1. Initial Checkout

Step	Control	Position/Operation	Observation
1	POWER	ON	RST indicator lit. Approximately ±10V square wave on CH1, dc level on CH2.
2	Dial	Rotate in both directions. Return to 2.0	Rotation ccw increases frequency of ⎍, rotation cw decreases frequency.
3	FREQUENCY MULTIPLIER	Press each button sequentially; return to ×1K	Frequency increases in decade steps, left buttons to right.
4	AMPLITUDE	Rotate ccw	Amplitude decreases.
5	DC OFFSET	Rotate cw. Return to OFF	Output immediately offset negative, then moves positive. OFF returns it to original level.
6	AMPLITUDE	Rotate cw	Square returns to original amplitude.
7	SWEEP RST	Release	Frequency increases as SWP OUT voltage increases.
8	FUNCTION	Press ∿ then ∿	Observe ∿ and ∿ waveforms.
9	MODE	Gate (depress CONT) (Remove VCG IN cable)	A dc level near zero volts.
10	MANUAL TRIGGER	Press and hold	Continuous ∿

Table 2-1. Initial Checkout (Continued)

Step	Control	Position/Operation	Observation
		Setup MARKER OUTPUT as a trigger source as shown in figure 2-2.	
11	TIME	FAST	
12	MARKER	Vary	Number of ∿ cycles gated varies with width of marker pulse.
13	MODE	Trigger (depress TRIG/GATE)	One ∿ cycle per trigger (marker pulse).
14	TIME knob	Vary	Number of triggered pulses vary as sweep generator period is varied.
		Remove cable from TRIG IN and MARKER OUTPUT. Sync scope on SYNC OUT signal.	
15	MODE	Continuous (release CONT)	
16	SWEEP	Sweep (depress ON/OFF)	Waveform frequency varies from low to high, rapidly resets to low, continuously. 189 RST and COMPL indicators lit as sweep starts and completes.
17	TIME	Slow sweep (release FAST/SLOW, knob at 12 o'clock)	Slow sweep.
18	SWEEP	Single sweep (depress SNGL)	Sweep stops at high end frequency. COMPL indicator lit.
19		Reset to start frequency (depress RST)	Frequency resets to sweep start frequency.
20		Single sweep (release RST)	Frequency sweeps. COMPL indicator lights when stop frequency is reached.
21		Continuous sweep (release SNGL)	Continuous sweep.

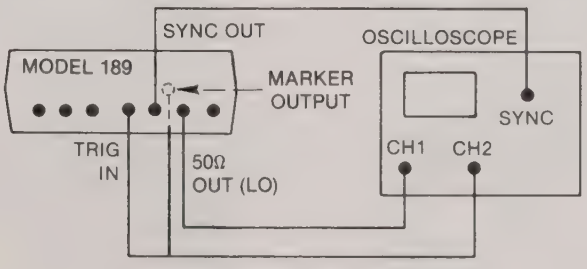


Figure 2-2. Second Setup

Table 2-1. Initial Checkout (Continued)

Step	Control	Position/Operation	Observation
22		Stop sweep (depress HOLD). Repeat several times. Release	Sweep stops instantly when hold is depressed.
23	LOG/LIN	Depress and release several times. Release	More sweep time spent at the lower frequencies when depressed (LOG).
		Change to setup shown in figure 2-3. Place scope in X-Y mode.	
24	TIME	Adjust for flicker free display.	
25	MARKER DURATION	Vary	Marker brightness varies.
26	Dial	Vary	Marker position varies.
27		1.0	Marker position. (This position is 1 kHz).
28	SET START	Press	Sweep starts at marker.
29	Dial	3.0	Note marker position. (This position is 3 kHz.)
30	SET STOP	Press	Sweep stops at marker.
31	Dial	4 . 0	189 MARKER OFF SCALE lit.
32	SWEEP SNGL	Depress	Sweep stops at stop frequency. COMPL indicator lights.
33	SWEEP RST	Depress	Sweep stops at start frequency. RST indicator lights.
34		Release	Sweep stops at stop frequency. COMPL indicator lighs.
35	SWEEP SNGL	Release	Sweep is continuous.
36	SWEEP HOLD	Depress and release several times.	Sweep stops at various positions in sweep interval. HOLD indicator lights.

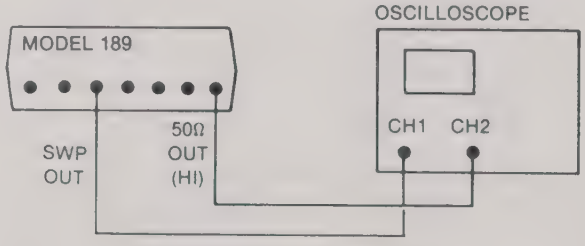


Figure 2-3. Third Setup

SECTION 3
OPERATION

3.1 CONTROLS AND CONNECTORS

Generator controls and connectors are shown in figure 3-1 and keyed to the following descriptions.

1 **FREQUENCY Dial**—Settings under dial index mark summed with **25** (if external voltage is applied) and multiplied by **3** determine the output frequency in any non-sweep mode. In sweep modes, the dial used to set start and stop frequencies and to set marker occurrence. Outer dial markings are used when in linear mode and inner markings when in logarithmic mode. Linear or logarithmic mode is determined by **2**.

2 **LOG/LIN Pushbutton**—Depressed button gives logarithmic distribution to output frequencies, whether the frequencies are determined by dial position, external voltage input or internal sweep ramp input. Released button gives linear distribution of output frequencies.

3 **FREQUENCY MULTIPLIER Pushbutton**—Selects one of seven frequency multipliers for **1** and **25**.

4,5 **MODE Pushbuttons**—The combination of depressed and released buttons gives continuous, trigger and gated modes. These modes are described here and illustrated in figure 3-2.

CONT—**4** released. Continuous output at **12** and **13**.

TRIG—**4** and **5** depressed. DC level output until generator is triggered by **6** or TTL level signal at **16**. When triggered, output is one cycle at generator frequency followed by the dc level.

GATE—**4** depressed and **5** released. As for TRIG except the output is continuous for the duration of manual or external trigger signal. The last cycle started is always completed.

6 **MAN TRIG Pushbutton**—Triggers or gates the output signal when generator mode is TRIG or GATE (ref: **4, 5**). In trigger mode, one waveform cycle is output when the button is pushed. In gate mode, waveform cycles are continuously output as long as the button is held in.

7 **FUNCTION Pushbuttons**—Selects sine (∿), triangle (∿), square (⊓) or when all three buttons are released, a dc level set by **9**.

8 **TIME Pushbutton and Knob**—Pushbutton selects FAST or SLOW sweep range and know varies the time within the selected range.

9 **DC OFFSET Knob**—Offsets the 50Ω OUT waveform or gives dc levels from −10V to +10V (−5V to +5V into 50Ω) at **12** HI 50Ω OUT and from −1V to +1V (−0.5V to +0.5V into 50Ω) at **12** LO 50Ω OUT. An OFF position ensures no dc offset. Single peak and offset is limited to ±10V (±5V into 50Ω). It may be necessary to reduce signal amplitude to prevent clipping when offset is used (ref: figure 3-3).

10 **AMPLITUDE Knob**—Ccw rotation reduces waveform amplitude at **12** by 30 dB. DC and offset voltages are not affected by this control.

11 **MARKER DURATION Knob**—Sets duration of the zero slope portion of the sweep ramp (ref: figure 3-2). Cw rotation increases marker duration and ccw rotation decreases marker duration. An OFF position disables the marker.

MARKER-OFF SCALE Indicator—Lights when the marker (dial) is not set between start and stop frequency.

12 **50Ω OUT**—The main outputs of the generator for the function selected. HI output, maximum is 20 Vp-p (10 Vp-p into 50Ω). LO output is 20 dB (1/10) lower in amplitude than HI output. Amplitude **10** gives 30 dB continuous variation of

the amplitude. The output source impedance is 50Ω. Peak output current for normal operation is 100 mA. Maximum short circuit current is 200 mA.

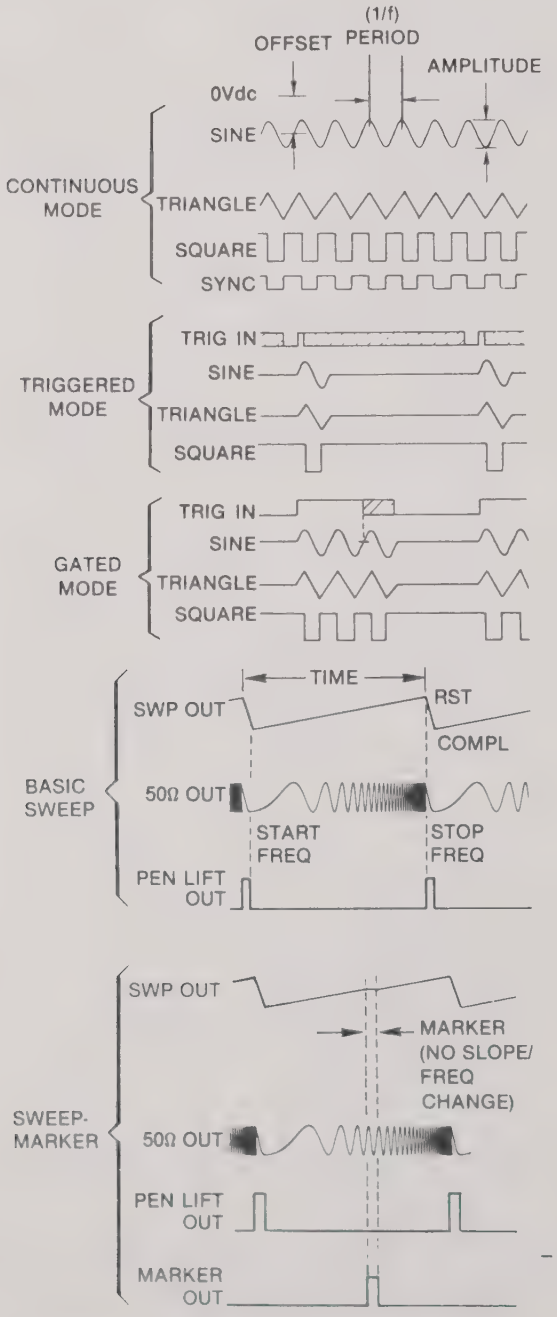
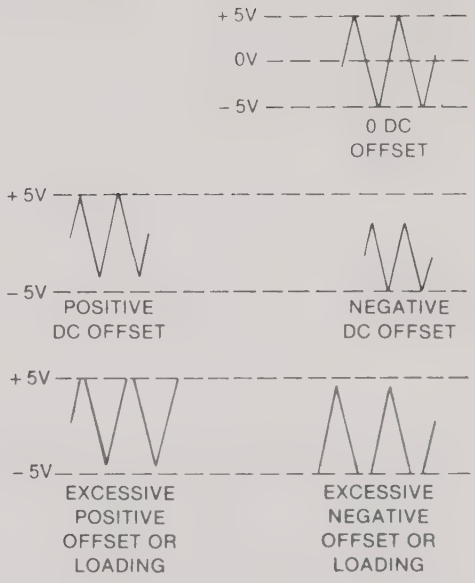


Figure 3-2. Waveform Characteristics



NOTE: Example is HI output into a 50Ω load.

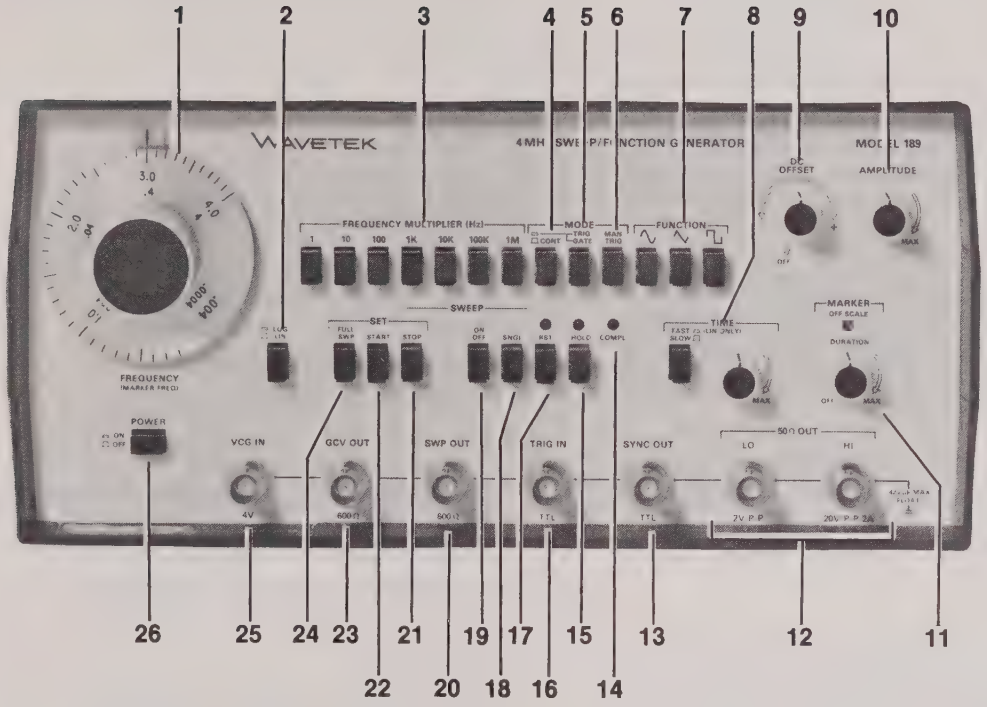
Figure 3-3. DC OFFSET Control

13 **SYNC OUT Connector**—Gives TTL square wave for each cycle of the generator. To be used for synchronization or as a TTL signal capable of driving 20 TTL loads.

14 **COMPL Indicator**—Lights when the sweep has reached stop frequency. When continuously sweeping, COMPL light will flash at a rate determined by TIME **8**. In single sweep (SNGL depressed, HOLD and RST extended), the COMPL indicator remains on after the sweep reaches the stop frequency.

15 **HOLD Pushbutton and Indicator**—Depressing the button or an external hold command at **29** instantaneously stops sweep and indicator lights. The sweep resumes and HOLD indicator goes out when button is extended or the external hold command at **29** is removed. (Also refer to **29**.1)

16 **TRIG IN Connector**—Accepts TTL signal to trigger or gate the generator. The generator triggers on the rising (low to high) transition and gates on during the positive (high) portion of the triggering signal.



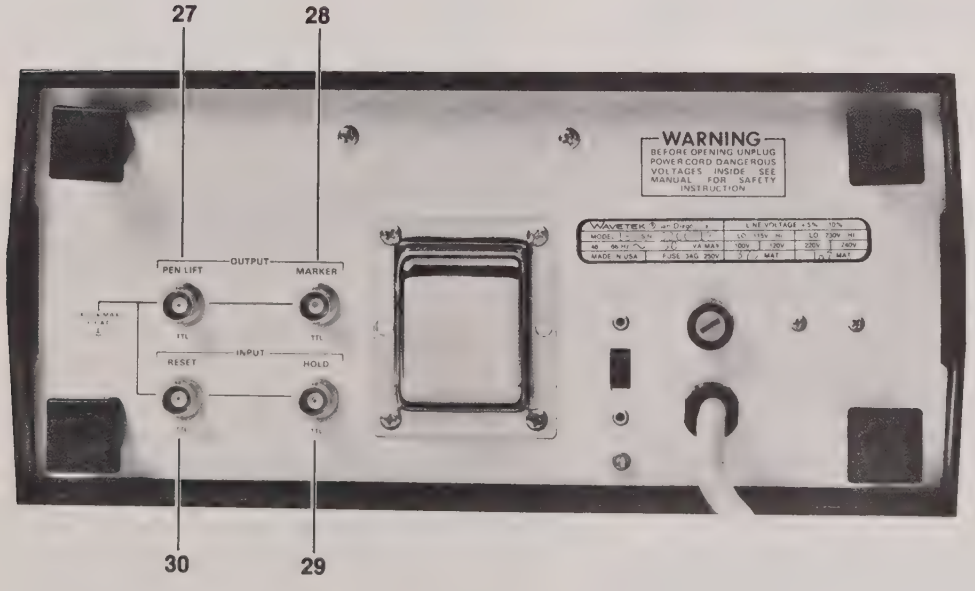


Figure 3-1. Controls and Connectors

17 **RST Pushbutton and Indicator**—Pushbutton depressed or a RST command at **30** instantaneously resets and holds sweep to the start frequency. The RST indicator lights to indicate the RST button is depressed. Extending the pushbutton or removing the external RST command from **30** initiates sweep from the start frequency and extinguishes the light. (Also refer to **30**.

18 **SNGL Pushbutton**—Selects single sweep. In this mode, releasing the RST button **17** or removing the external command at **30** initiates the sweep. RST and COMPL indicators show sweep status.

19 **SWEEP ON/OFF Pushbutton**—Extended selects the unsweep operation: the frequency is set by **1, 3** and **25**. Depressed selects sweep from start to stop frequencies (ref: **21, 22** and **24**).

20 **SWEEP OUT Connector**—Supplies a 0 to 4V open circuit ramp with a momentary zero slope for the duration of the marker (ref: **1** and **11**). Sweep output source impedance is 600Ω.

21 **SET STOP Pushbutton**—Pressing sets the stop frequency to that frequency selected by frequency dial **1**.

22 **SET START Pushbutton**—Pressing sets the stop frequency to frequency selected by frequency dial **1**.

23 **GCV Connector**—Provides a 0 to 4V open circuit output proportional to frequency of main generator. For use as a horizontal drive signal.

24 **FULL SWEEP Pushbutton**—Selects a full sweep of the selected frequency range. Frequency is from 0.004 to 4 linear mode (or 0.0004 to 4, log mode) multipied by the selected multiplier **3**. Frequency change is 1000:1 for linear sweep or 10,000:1 for logarithmic sweep.

25 **VCG IN Connector**—Accepts ac or dc voltages to proportionately control frequency within the range determined by the frequency multiplier **3**. Positive voltage increases the frequency set by the dial **1**; negative voltage decreases the frequency. The VCG IN will not drive the generator frequency beyond the normal dial limits of a range. Input impedance is 2 kΩ.

26 **POWER Pushbutton**—Depressed turns the generator ON, extended OFF.

The following connectors are located on the rear panel.

27 **PEN LIFT OUTPUT Connector**—Provides a momentary TTL high (or low if altered) during reset interval or whenever the sweep is stopped except during marker interval.

28 **MARKER OUTPUT Connector**—A TTL level high for duration of marker (ref: **11**).

29 **HOLD Connector**—An input (TTL low or contact closure) or depressing the HOLD button **15** stops the sweep at an instantaneous frequency and lights the HOLD indicator **15**. When the hold is released, the sweep continues and the indicator extinguished. Also refer to **15**.

30 **RESET Connector**—An input (TTL low or contact closure) or depressing the RST button **17** causes the generator to instaneously reset to the start frequency and the RST indicator **17** to light. When the reset is released the sweep begins at the start frequency and the RST indicator extinguishes. Also refer to **17**.

3.2 OPERATION

Perform the initial checkout in Section 2 for the feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.1.

3.2.1 Signal Termination

Proper signal termination, or loading of the generator connectors is necessary for its specified operation. For example, the proper termination of either of the 50Ω OUT connectors is shown in figure 3-4. Placing the 50Ω terminator, or 50Ω resistor in parallel with a higher impedance matches the receiving instrument input impedance to the coax characteristics and generator output impedance, thereby minimizing signal reflection or power loss on the line due to the impedance mismatch.

The input and output impedances of the generator connectors are listed as follows:

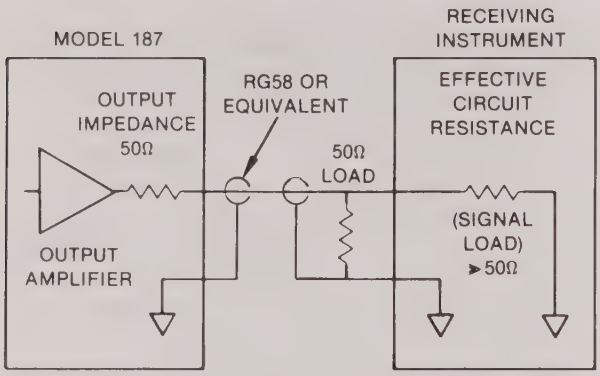


Figure 3-4. Signal Termination

Connector	Impedance
50Ω OUT (HI)	50Ω
50Ω OUT (LO)	50Ω
SYNC OUT (TTL)	**
TRIG IN	*
SWP OUT	600Ω
GCV OUT	600Ω
VCG IN	2 kΩ
PEN LIFT OUT (TTL)	*
MARKER OUT (TTL)	*
RESET INPUT	*
HOLD INPUT	*

* The TTL OUT connectors can drive up to 5 Transistor-Transistor-Logic (TTL) loads (low level between 0V and 0.4V and high level between 2.4V and 5V). They should not be connected to resistive loads less than 6000Ω. The TTL input connectors accept TTL logic levels, are diode protected and require 500 μA drive.

** SYNC OUT is diode protected and can drive up to 20 TTL loads.

3.2.2 Manual Function Generator Operation

For basic operation, select the waveform frequency and amplitude. The following steps demonstrate manual control of the function generator. (Bold numbers are keys to figure 3-1.)

Step	Control/Connector	Setting
1	50Ω **12**	Connect circuit to either output (refer to paragraph 3.2.1).
2	FREQUENCY MULTIPLIER **3**	Set to obtain desired range of frequency.
3	LIN/LOG **2**	As desired.
4	FREQUENCY Dial **1**	Set to desired frequency within the range.
5	SWEEP ON/OFF **19**	Extended.
6	FUNCTION **7**	Set to desired waveform.
7	DC OFFSET **9**	Set as desired. Limit waveform amplitude to prevent clipping (see figure 3-2).
8	AMPLITUDE **10**	Set for desired amplitude.

3.2.3 Voltage Controlled Function Generator Operation

Operation as a voltage controlled function generator (VCG) is as for a manually controlled function generator, only the frequency within a particular range is controlled by an external voltage (±4V excursions) injected at the VCG IN connector. Perform the steps given in paragraph 3.2.2, only set the frequency dial to determine a reference from which the frequency is to be voltage controlled:

1. For frequency control with positive dc inputs at VCG IN, set the dial for a lower frequency limit.

2. For frequency control with negative dc inputs at VCG IN, set the dial for an upper frequency limit.

3. For modulation with an ac input at VCG IN, set the dial at the desired center frequency. Do not exceed the limits of the selected frequency range.

NOTE

Nonlinear operation may result when the VCG input voltage is excessive; that is,when the attempted generator frequency exceeds the range limits. The upper limit is four times the multiplier setting, and the lower limit is 1/1000th (linear) or 1/10,000 (logarithmic) of the upper limit.

Figure 3-5 is a nomograph with examples of dial and voltage effects. Example 1 shows that with 0V VCG input, frequency is determined by the main dial setting,

2 (linear mode) or .04 (logarithmic mode) in this example. Example 2 shows that with a positive VCG input, output frequency is increased. Example 3 shows that with a negative VCG input, output frequency is decreased. (Note that the Output Frequency Factor column value must be multiplied by a frequency range multiplier to give the actual output frequency.)

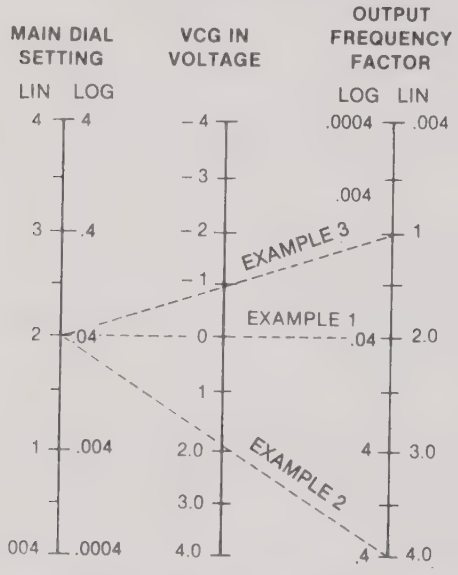


Figure 3-5. Voltage Controlled Function Generator Operation

The up to 1000:1 (linear) or 10,000:1 (logarithmic) VCG sweep of the generator frequencies available in each range results from a 4V excursion at the VCG IN connector. With the frequency dial set to 4.0, excursions between −4V and 0V at VCG IN provide the up to 1000:1 (lin) or 10,000:1 (log) frequency sweep. With the dial set to .004 (linear) or .0004 (logarithmic), excursions between 0V and +4V at the VCG IN provide up to 1000:1 (linear) or 10,000:1 (logarithmic) sweep within the set frequency range.

3.2.4 Sweep Generator Operation

Operation as a sweep generator is similiar to manual controlled generator operation except the main generator operation can be linearly or logarithmically swept between two selected frequencies. In addition, the 189 may be used as a single sweep generator. In either mode, the main dial can serve as a calibrated marker.

3.2.4.1 Basic Sweep Operation

Operation as a recurring sweep generator is described below and illustrated in figure 3-2. Primary settings are discussed in paragraph 3.2.2.

Step	Control	Setting
1	MODE: CONT **4**	Press to release (continuous mode of the main generator is necessary for sweep mode).
2	SNGL **18**	Extended
3	RST **17**	Extended
4	HOLD **15**	Extended
5	MARKER DURATION **11**	OFF
6	SWEEP ON/OFF **19**	Depresed ON
7	SET FULL SWP **24**	Press for full range sweep. Full sweep for logarithmic is 10,000:1.
8	SET START **22**	Set frequency dial **1** to desired start frequency (frequency may be greater or less than stop frequency). Press START.
9	SET STOP **21**	Set frequency dial **1** to desired stop frequency (frequency may be less or greater than start frequency). Press STOP.
10	TIME **8**	Set range and knob for desired sweep rate.
11	LIN/LOG **2**	As required.
12		Set up scope in X-Y mode using either SWP OUT or GCV OUT for X-axis.

3.2.4.2 Single Sweep Operation

Operation as a single sweep generator is just slightly different than basic sweep operation. Primary settings

are as described in paragraph 3.2.2 and 3.2.4.1. Steps peculiar to single sweep operation are:

Step	Control	Setting
1	SNGL **18**	Depress (COMPL indicator will light).
2	RST **17** (or **30**)	Pushbutton: depress. (Connector: TTL low or contact closure.)
3	RST **17** (or **30**)	Pushbutton: release. (Connector: TTL high or open contact.)

3.2.4.3 Sweep Marker Operation

Operation as a sweep generator with marker requires an oscilloscope with X-Y inputs. Because the instantaneous SWP OUT voltage is proportional to the generator frequency, the setup of figure 3-6 gives a display of frequency (X axis) vs amplitude (Y axis). A constant SWP OUT ramp slope gives a linear distribution of the scope's electron beam across the scope display; however, the zero slope spot on the ramp, which is the frequency marker, gives a momentary pause to the beam and creates a bright spot, a marker. The width of the zero slope spot is adjustable by the MARKER DURATION knob and the position of the marker is adjustable by the FREQUENCY dial. The dial reading is the frequency position of the displayed marker. Primary settings for sweep marker operation are described in paragraph 3.2.2 and 3.2.4.1. Steps peculiar to sweep marker operations are:

Step	Control	Setting
1		Connnect equipment as shown in figure 3-6.
2	MARKER DURATION **11**	ON (vary duration for marker brightness on scope).

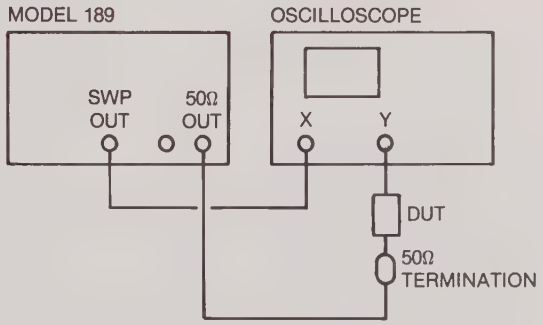


Figure 3-6. Sweep Marker Setup

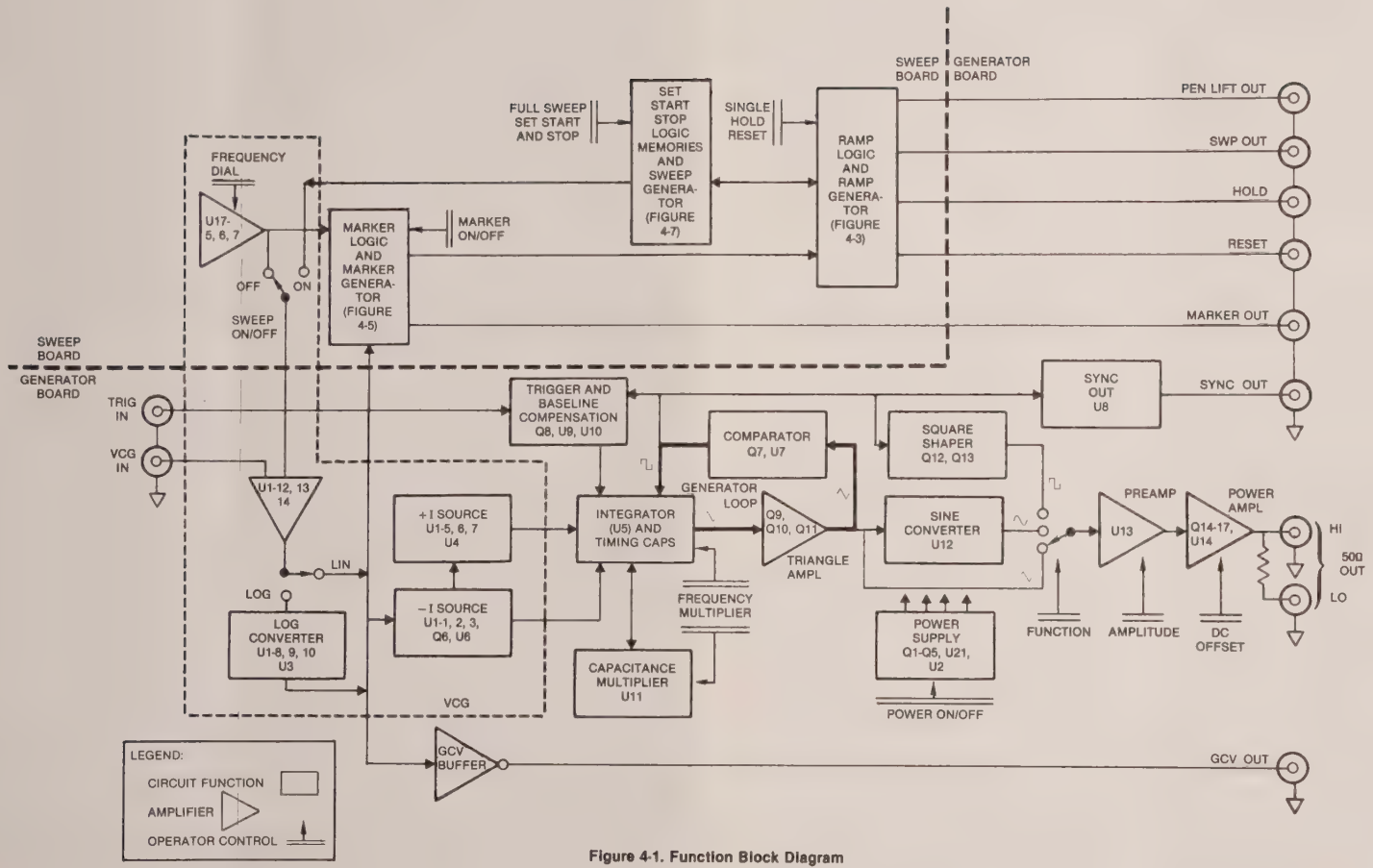


Figure 4-1. Function Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

This section describes the functions of major circuit elements and their relationships to one another as shown in figure 4-1, functional block diagram.

4.2 GENERATOR BOARD

As shown in figure 4-1, with sweep off the VCG (Voltage Control of Generator) sums voltage inputs from the dial buffer located on the sweep board and the VCG IN signal, if any. This sum voltage controls the magnitude of a complementary current source and current sink. This current varies linearily from approximately 2 mA to 2 μA over a 1000:1 (4.0 to 0.004) range or logarithmically from approximately 2 mA to 2μA over a 10,000:1 (4.0 to 0.0004) range of each frequency multiplier. The VCG also controls a trigger baseline compensation circuit. The sum voltage (called GCV, Generator Control Voltage) is also fed to sweep circuits (ref: paragraph 4.3)

The integrator, consisting of the bridge diodes and timing capacitors, is switched by the comparator output. This switching causes either the current source or current sink to charge the timing capacitor selected by the frequency multiplier. When the current source is switched in, the charge on the timing capacitor will rise linearily, producing the positive-going triangle slope. Likewise, the current sink produces the negative-going triangle slope.

The triangle amplifier is a unity gain amplifier whose output is fed to the comparator and to the output circuits. The comparator operates as a window detector with limit points set to the triangle peaks. The $\pm$2V output is sent back to the integrator and timing capacitor. When the output is $+$2V, the triangle is positive-going until the $+$1.25V limit is reached and the comparator output switches to $-$2V. When the output is $-$2V, the triangle is negative-going until the $-$1.25V limit is reached and the comparator output switches back to $+$2V, repeating the process. In this manner, the basic function generator loop, the bold path in figure 4-1, produces simultaneous generation of triangle and square waves at the same frequency.

The output frequency is determined by the magnitude of the timing capacitor selected by the frequency multiplier switches and by the magnitude of the currents supplied to and removed from it. Since the currents are linearily proportional to the sum of the VCG inputs, so will be the output frequency.

To extend the lower frequency capability of the generator, a capacitance multiplier circuit divides VCG currents by 10 (effectively multiplying the timing capacitor by 10) for each of the lower 3 multiplier ranges.

The TTL square from the comparator is buffered and sent to the SYNC OUT TTL connector. The other side is sent to the trigger flip-flop and to a level shifter to produce the $\pm$2V bipolar square for the diode gate and the square shaper circuits. The square shaper converts the square into a current signal and applies it to the $\sqcap\!\!\sqcup$ FUNCTION switch. The buffered triangle is applied to the $\wedge\!\!\vee$ FUNCTION switch and to the sine converter input. The sine converter, using the nonlinear characteristics of its diodes, converts the triangle into a sinusoidal current for the $\wedge\!\!\vee$ FUNCTION switch.

The selected function is sent to the preamplifier, where it is inverted and buffered. The preamplifier output goes to the output amplifier through the AMPLITUDE control where it is summed with offset voltage from the DC OFFSET control. Here, waveform and offset are inverted and amplified to a 10V peak signal which can drive a 50Ω termination from a 50Ω source impedance. The output amplifier drives the 50Ω OUT HI connector and a resistor divider to produce the 50Ω OUT LO output.

Noncontinuous modes of operation (trigger and gate) result from allowing or preventing the VCG current source from charging the timing capacitor. Whenever the trigger flip-flop output is low, each of the two trigger diodes conduct a current I, sourcing 2 I to the baseline compensation circuit. This removes the current I from the VCG current source and forces a 0V baseline at the triangle amplifier input.

When the CONT switch is released, trigger logic is inhibited from passing any trigger signals and the trigger flip-flop output is held high. This prevents the trigger diodes from conducting and the generator loop operates continuously.

When the CONT switch is pressed, the generator loop is held at the 0V baseline. Pressing the TRIG/GATE switch puts the instrument in triggered mode and any external or manual trigger signals at the trigger logic input will be transformed into a narrow pulse corresponding to the low-to-high transition of the trigger input. This pulse sets the trigger flip-flop high and allows the generator loop to run. When the triangle negative peak is reached, the comparator low-to-high transition clocks the trigger flip-flop low and, when the 0V baseline level is reached, the generator loop again stops. The result is a single cycle generated after the triggering signal corresponding to 0 to 360° of phase. Successive triggered waveforms always start at the same 0° point.

Releasing the TRIG/GATE switch puts the instrument in the gated mode. This is identical to the triggered mode, except the trigger flip-flop is held high for the full duration of the triggering signal. The generator produces continuous waveforms during the time the external signal is high or the manual trigger switch is held in. The last triggered cycle started is always completed and successive gated bursts always start at the 0° point.

4.3 SWEEP BOARD

When in sweep mode, the generator board receives a ramp as the VCG signal to sweep the frequency of the instrument output. Notice (figure 4-2) that the frequency dial no longer controls the output frequency. Instead, the dial is connected to two comparator circuits; one is montored by the marker generator when the MARKER is on and the other is montored by the start or stop memory when SET START or STOP are pressed, respectively.

When MARKER is on, the dial position is monitored by the marker generator which controls the position of pause in the ramp voltage. This dwell causes the instrument output to momentarily remain at the "marked" frequency and can be detected as bright line on a monitoring oscilloscope.

When SET START or STOP are pressed, the dial position is monitored by the respective start or stop memory and equivalent information is stored, which alters the start and stop levels of the sweep ramp.

The sweep board discussion considers three major blocks and their control logic as shown in figure 4-2. The blocks are:

Ramp Generator and Control Logic. This is a 0 to +4 volt ramp generator with circuitry to force three modes of condition: hold, single, or reset. These modes cause the sweep of the main generator to: hold at one frequency, sweep once to top of sweep rrequency and hold, or sweep and reset to start of the sweep frequency, respectively. This generator is therefore the reference of the sweep board. Any of the three conditions forced on the ramp are modified by the sweep generator and passed to the main generator when sweep is on. The 0 volt level of reset always corresponds with the start sweep frequency and the +4 volt level of single sweep always corresponds with the stop sweep frequency. Hold will place the ramp at any value between 0 and +4 volts inclusive. this ramp and forced modes of condition go to the front panel SWP OUT BNC, and continue to run whether or not the sweep is on. SWP OUT can therefore be used independently of the main generator.

Marker Generator and Control Logic. The marker generator is a "timed hold" control to the ramp generator. When engaged, the marker generator stops and holds the sweeping reference ramp on a point which corresponds to the desired marker frequency. When the marker times out, the ramp generator completes the sweep. This "timed hold" is repeated on each subsequent sweep. The marker generator, like the ramp generator runs whether the sweep is on or off. However, if the sweep is off, the marker generator is triggered into action by the reset pulse of the ramp, thus allowing a variable time delay before the beginning of each sweep. This feature allows the SWP OUT to gate the main generator for a burst mode, if desired.

Sweep Generator and Control Logic. The 0 to +4 volt ramp is fed to two digitally controlled three decade attenuators and summing DAC's, which modify the start and stop levels of the ramp. This circuitry enables the modified ramp to sweep up or down. When sweep is on, the modified ramp is fed to the VCG of the main gnerator. Digital memories set by the set start/stop buttons control the DAC's.

The control logic, while engage, is the master controller of the whole sweep board. This logic coordinates the ramp generator, sweep generator, memories, and dial to produce the final sweeping results.

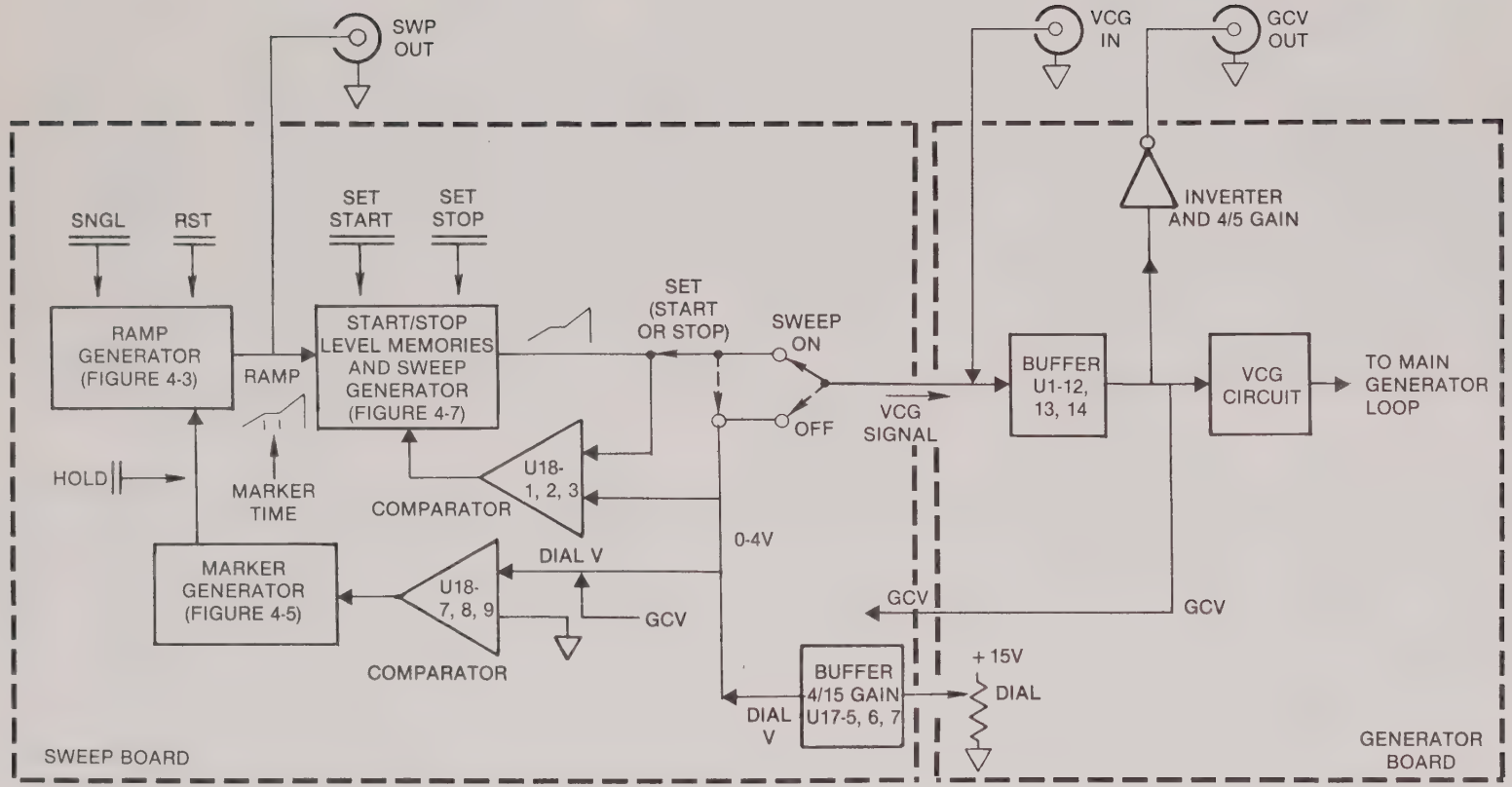


Figure 4-2. Sweep

4.3.1 Ramp Generator and Ramp Control Logic

Refer to figures 4-3 and 4-4 and schematic 0103-00-0867 (sheet 1) while reading this description. With the sweep on, transistors Q2 and Q3 form a variable con stant current source adjustable from 0.4 mA to 66 nA. To generate the 0 to 4 volt ramp, the current is switched via Q5 into C7 or the parallel combination of C7 and C8, which charge at a linear rate, creating the ramp. This ramp is then buffered and sent to the end-of-sweep comparator U23 (pins 1, 2, 3).

When the ramp voltage at pin 2 exceeds the reference +4 volts on pin 3, the comparator toggles from a logic high to a logic low. This logic low is then applied to the ramp reset circuitry, inverted and directed to set Q6 into conduction. Q6 conducting shorts the voltage on the charging capacitor(s). The logic low is also directed through the ramp stop circuitry which sets Q4 into conduction, thus diverting the constant current source away from the charging capacitor(s). The duration time that the comparator stays in reset is determined by the RC time constant of C15 and R57 in fast sweep and C15, C16 and R57 in slow sweep. Once the reset time of approximately 8 μs in fast sweep and 700 μs in slow sweep has passed, the comparitor goes back to a logic high, effectively removing the shorting Q6 and switching the constant current back into the timing capacitor(s). Thus a new cycle begins. Note that the comparator output also feeds U22 pin 2 for the pen lift BNC on the rear panel.

The ramp control logic circuitry not only helps to generate the ramp, but also forces three possible conditions on the 0 to 4 volt ramp. these three possible conditions are also present when selecting sweep start, sweep stop, full sweep, and marker. However, the immediate discussion will be limited to the single-sweep, hold, and reset controls.

In single sweep mode, the ramp charges to +4 volts, toggles the detector as in full sweep, but the detector output now is switched into the ramp +4 volt circuitry. Q7 is turned on and the +4 volt reference is applied to the timing capacitor to eliminate any drift. Note that the EOS time constant circuitry is effectively removed by placing a +5 volts on CR7 in the feedback path of U23 (pins 1, 2, 3) and by disconnecting the ramp reset circuit.

In reset mode, the ramp detector is held at a logic low, initiating a ramp stop condition. This stop condition causes Q4 to divert the constant current and Q6 of the ramp reset circuitry to short any voltage out of the timing capacitor(s). Thus the ramp is held at zero volts.

In hold mode, only Q4 is turned on. Thus the constant current is switched out of the timing capacitor(s) and into the current sink Q8 of the marker generator. The voltage level in the sweep ramp remains at a value between 0 and 4 volts until the current source is switched in to complete the +4 volt ramp.

Basically, the marker generator is a timed hold control. (When the sweep output is applied to a scope horizontal (X-axis) input, this hold or pause causes an intensified zone to appear on the display that corresponds to the marker frequency.)

4.3.2. Marker Generator and Control Logic

Refer to figure 4-5, schematic 0103-00-0867 (sheet 1) and Timing Sequence Diagram, figure 4-4, while reading this description. To trigger the hold function, the marker start comparator U18 (pins 5, 6, 7) sums a minus sweeping GCV with a stationary dial voltage. When the summing voltage at pin 5 equals 0, U18 toggles. It can toggle either high or low depending on whether the GCV is sweeping up or down. Marker U5 start/stop logic (pins 11, 12, 13) and U12 are used to change this altering pulse level to a unipolar pulse of a low level whose leading edge will correspond to the toggling of U18.

The leading edge from U12 then resets U5 (pins 1, 2, 3, 5), causing the normal shorting transistor Q8 to shut off and to set the Ramp Stop circuitry. Q4 now switches the constant current into either the fast or slow range charging capacitor(s). This charging or marker ramp voltage is then buffered and applied to U23 (pins 5, 6, 7). When the marker ramp voltage exceeds the variable voltage from duration pot R51 applied to pin 6, U 23 toggles high.

U23's high then sets U19 (pins 2, 3, 4), U5 (pins 1, 2, 3) and U19 (pins 11, 12, 13). all this setting does the following. Shorting-transistor Q8 comes on , discharging the marker timing capacitor(s), ramp stop goes off causing Q5 to switch the charging current back into the sweep ramp, and finally a logic high is kept on the cathode of the off-scale diode.

Since the same constant current is used to cnarge both the sweep ramp capacitors and the marker ramp capacitor, the charging marker generator is directly proportional to the sweep ramp. Hence, the marker duration will always be from 2% to 65% of the sweep ramp time.

If there had not been a marker comparison because the dial voltage was out of range to the sweeping negative GCV, U19 (pins 11, 12, 13) would have placed a logic low on the off-scale diode causing the LED to light. Without the set pulse of U23 (pin 7), U19 remains in reset mode, so placed there from the reset pulse of the sweep ramp.

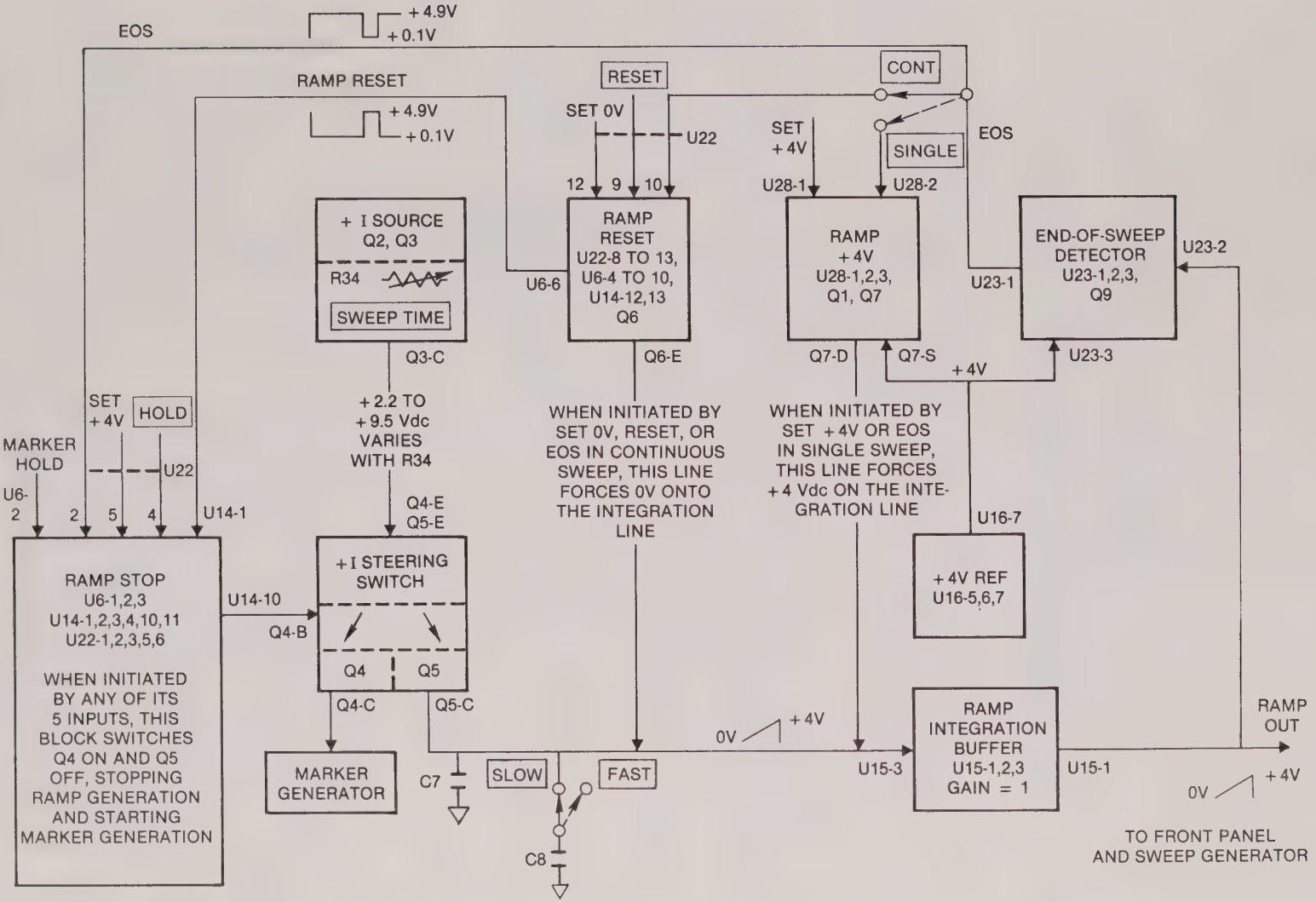


Figure 4-3. Ramp Generator Block Diagram

FRONT PANEL SETUP: FREQUENCY DIAL: 2.0
MARKER: ON
MARKER DURATION: MAX
SWEEP TIME: FAST

NOT ALL GATES SHOWN — ONLY FUNCTIONAL INPUT/OUTPUTS.
WAVEFORM IS REPETITIVE — THE EOS LOW PULSE IS A ONE-SHOT MULTIVIBRATOR WHICH RESETS HIGH AFTER A FIXED DELAY.

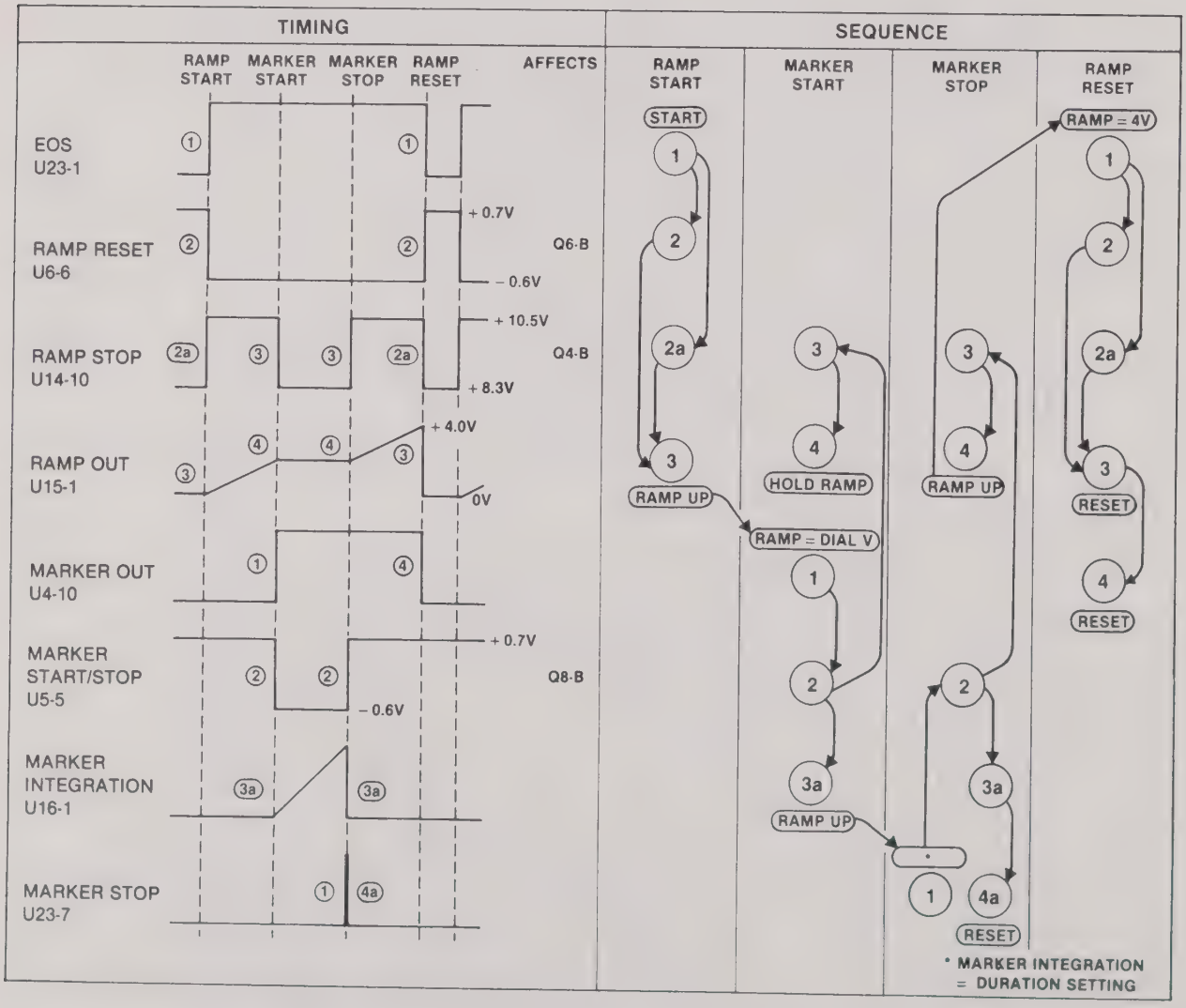


Figure 4-4. Ramp/Marker Generation Timing/Sequence Diagram

Ramp Start

1 Ramp reset goes high.

2 The high from U23-1 causes U22-8 to go low. The low causes U6-8 to go high. The high causes U6-6 to go low. This removes Q6 transistor from the ramp generation.

2a The high from U23-1 causes U22-6 to go low. The low is inverted by U14-4. The resulting high causes U6-3 to go low. This is inverted by U14-10. The high from U14-10 causes Q4 current drain to turn off and Q5 to turn on.

3 As a result of 2 and 2a the timing capacitor(s) begin to charge up. This can be measured at U15-1.

Marker Start

1 The dial voltage + the ramp V = 0 at U18-5. This causes U18-7 to go high if sweeping up or low if sweeping down. U18-7 causes U4-10 to go low (if sweeping up) or high (if sweeping down). This high or low pulse is converted into a negative pulse by U5-7, 9 11, 12 and U12. The negative pulse feeds U5-1.

2 As a result of **1**, U5-5 goes low. This causes shorting transistor Q8 to go off.

3 U5-5's low causes U6-3 to go high. This high is inverted by U14-10. The high from U14-10 causes switching transistor Q4 to come on.

3a As a result of **3** the marker generator ramp begins charging.

4 As a result of **3** the ramp out stops charging.

Marker Stop

1 Marker ramp voltage U13-5 is greater than U23-6 duration voltage. This causes U23-7 to toggle high.

2 The high from U23-7 causes U4-13 to go low. The low from U4-13 causes U19-5 to go high. U19-5's high causes U4-4 to go low. The low sets U5-5. The Q of U19-6 goes low setting U19-10. This keeps the off-scale diode from lighting.

3 The high from U5-5 causes U6-3 to go low. This low is inverted by U14-10. The high from U14-10 turns Q4 off.

3a The high from U5-5 causes shorting transitor Q8 to turn on and drains the marker capacitor.

4 With Q4 off and Q5 on, ramp out as measured at U5-1 charges up.

4a As a result of U16-1 going low U23-7 returns to low level.

Figure 4-4. Ramp/Marker Generation Timing/Sequence Diagram (Continued)

Ramp Reset

1 U15-1 charges past +4.0V. This causes comparator U23-1 to go low. The time U23-1 stays low is determined by RC time constants C15, C16, and R57.

2 U23-1's low causes U22-8 to go high. U22-8's high causes U6-8 to go low. U6-8's low causes U6-6 to go high. U6-6's high causes shorting transitor Q2 to discharge the charging capacitor's voltage.

2a U23-1's low causes U6-3 to go high. This high is inverted by U14-10. U14-10 causes current diverter Q4 to turn on. This directs the current to shorting transistor Q8.

3 As a result of Q6 and Q4 being on, ramp capacitor(s) are discharged to 0 volts. This causes the output buffer U15-1 to be at 0 volts.

4 The low from U15-1 causes a difference voltage between dial volts and sweep ramp. This causes U4-10 to go high.

Figure 4-4. Ramp/Marker Generation Timing/Sequence Diagram (Continued)

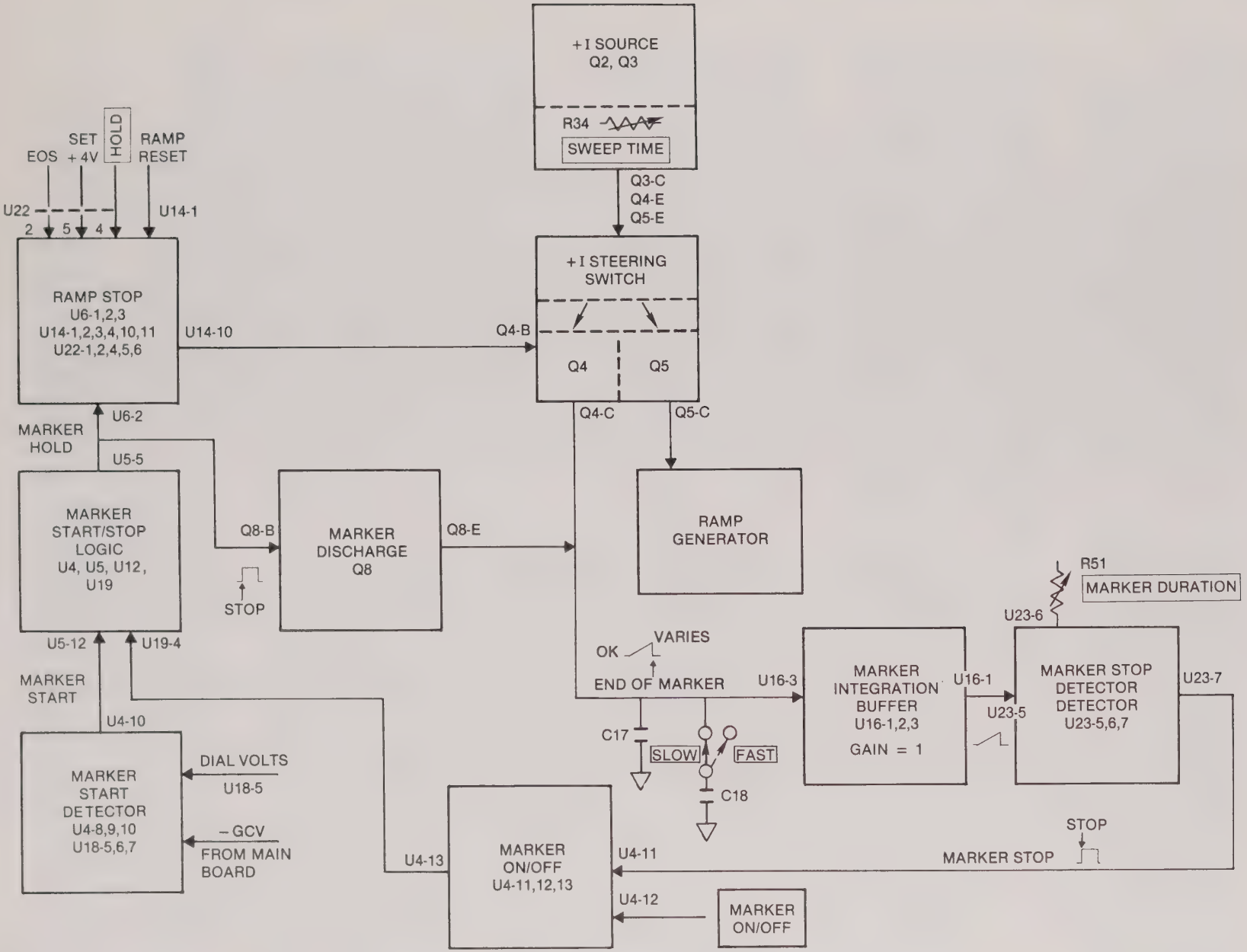


Figure 4-5. Marker Generator

Finally, if the sweep is off, the 0 to +4 volt ramp and marker still run. The marker, however, is now triggered by the reset pulse of the ramp generator, thus causing the marker to affect the time delay before the beginning of each sweep. Circuitry involved in the triggering is SW6-A, which places +5 volts on U12 (pin 13) and the output of U14 (pin 4), which sends the reset pulse to U12 (pins 12, 5, 9).

4.3.3 Sweep Generator and Control Logic

Refer to figure 4-6 for the summing principle of the sweep generator. The figure shows two ramps, one the reverse of the other. Each has its own slope and amplitude but the periods are the same. The subsequent summing of the ramps results in an output ramp that starts at the height of the bottom ramp and ends at the height of the top ramp. This is the summing principle the sweep generator works upon.

Now refer to figure 4-7 and schematic 0103-00-0867, sheet 2. Output of the start DAC (U8) with attenuator (Q12, Q13) generates a current ramp that begins at the desired frequency and sweeps to 0 amps while the output of the stop DAC (U1) with attenuator (Q10, Q11) sweeps from 0 amps to the current value equal to the desired stop frequency. These current ramps are then summed at the input of U17 pin 2 and the output voltage of U17 pin 1 is the quivalent of a sweeping dial VCG signal of the desired start and stop frequency. Since the buffered dial voltage is 0 to +4 volts, the sweeping output will be between 0 to +4 volts or, when in full sweep, the full 0 to +4 volts inclusive.

The reference ramp generator feeds the DAC's and attenuators. This reference is inverted (changed to +4 to 0 volts) before being processed by the start DAC with attenuator. The two sets of attenuators and DAC's change the start level of the inverted reference ramp to the proper start VCG (output of U17 pin 1) and change the stop level of the noninverted reference sweep to the proper stop VCG (output U17 pin 1). In this context, the DAC's are used as a data controlled gain amplifier.

The DAC's amplify any ramp fed to them from 0 gain to approximately 2/5 unity gain with 255 divisions of gain between. The attenuators that precede both DAC's divide the reference ramp and it's inversion by one of three decades (divide by 1, 10, 100). The decade used by either DAC is dependent upon whether the instantaneous frequency selected in start or stop is set from approximately 4 to .4 on the dial (divide by 1), set from .4 to 0.04 on the dial (divide by 10), or is set from 0.04 and down on the dial (divide by 100). Each decade, after being amplified to compensate for the decrease in DAC unity gain, has 0 to 255 bits of gain available to generate a matching voltage to the instaneous start or stop dial voltage within the decade. This three decade technique allows the setting of a start or stop frequency to have a resolution of 0.4% or better within any decade.

Associated with the start DAC attenuator and the stop DAC attenuator are their respective memories. The 8 bit DAC memories (U2, U9) and the 2 bit attenuator memories (U10, U11) store digital information that controls both ramp outputs for summing. By storing information in the memories, and using the digital information to generate the proper sweeping VCG signal, the dial is free to be used as a marker. The process of setting the memories to the proper digital byte, involves activiating the control logic.

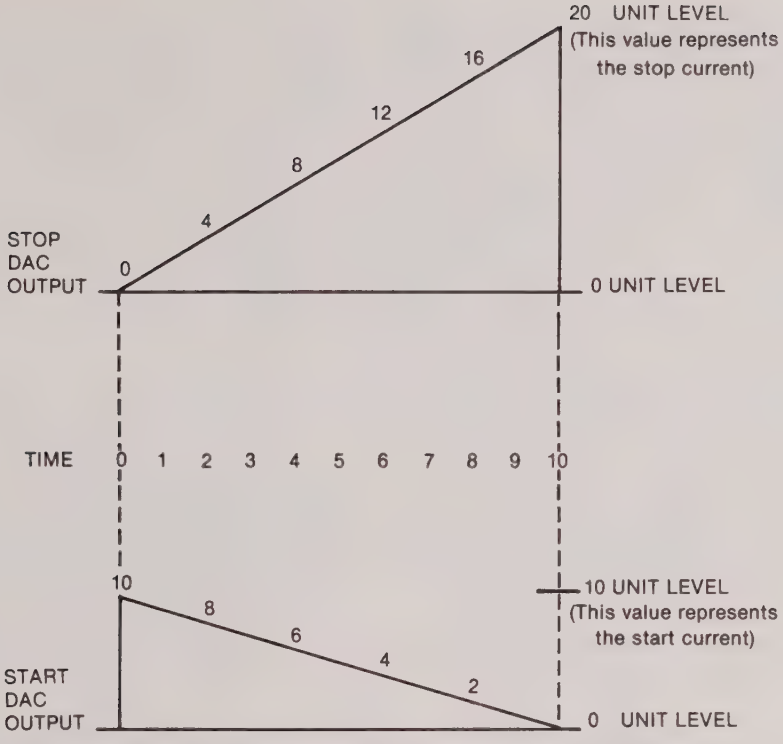
There are four phases of action the control logic must accomplish to set the memories to the proper digital information. These phases control the whole sweep board and give a picture of the total functioning sweep system. In full sweep mode, the logic circuitry automatically sets the memories to produce a full sweep. In set start or set stop mode, specific start and stop frequencies are desired by the user, so the action of the logic is similiar but different. The analysis will therefore describe the action of the full sweep first, and a hypothetical start/stop situation last.

The object of pressing FULL SWP is to have the sweep generator sweep the VCG circuit of the main generator from 0 to +4 volts. Since 0 to +4 volts is the condition of the unattenuated, full-count stop ramp, full sweep condition will achieve this and keep the start ramp at zero. The ramp sum will then allow a full sweep, 0 to +4V VCG signal. By pressing FULL SWP, three of the four phases of control logic are initiated to set the memories. The last phase occurs a fixed time after the release of the full sweep button.

Phase 1 prepares the memories to be set to the proper digital value. The three steps of this phase are:

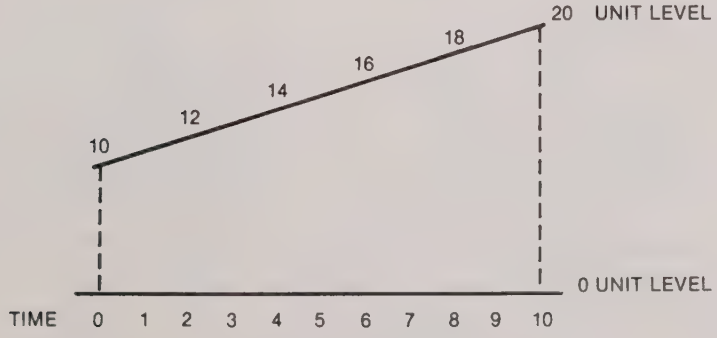
1) The stop attenuator 2 bit memory (U10) is reset to 0 which causes the attenuator to divide by 1. (This attenuator setting, divide by 1, is correct when the stop frequency is in the upper part of the dial which it is.)

2) The start 8 bit memory (U9) and the stop 8 bit memory (U2) are reset to 0 for 0 gain. This causes both the start and stop DAC to have 0 amp output at this moment.



BY SUMMING BOTH OF THESE RAMPS A SINGLE RAMP IS PRODUCED.

STOP DAC OUTPUT	0	4	8	12	16	20
	+	+	+	+	+	+
START DAC OUTPUT	10	8	6	4	2	0
SUMMED OUTPUT	10	12	14	16	18	20



NOTE
TIME AND CURRENT UNITS ARE NOT DEFINED.
THIS DIAGRAM DEMONSTRATES CONCEPT AND
DOES NOT REFLECT ACTUAL MEASUREMENT.

Figure 4-6. Summing Principle of the Sweep Generator

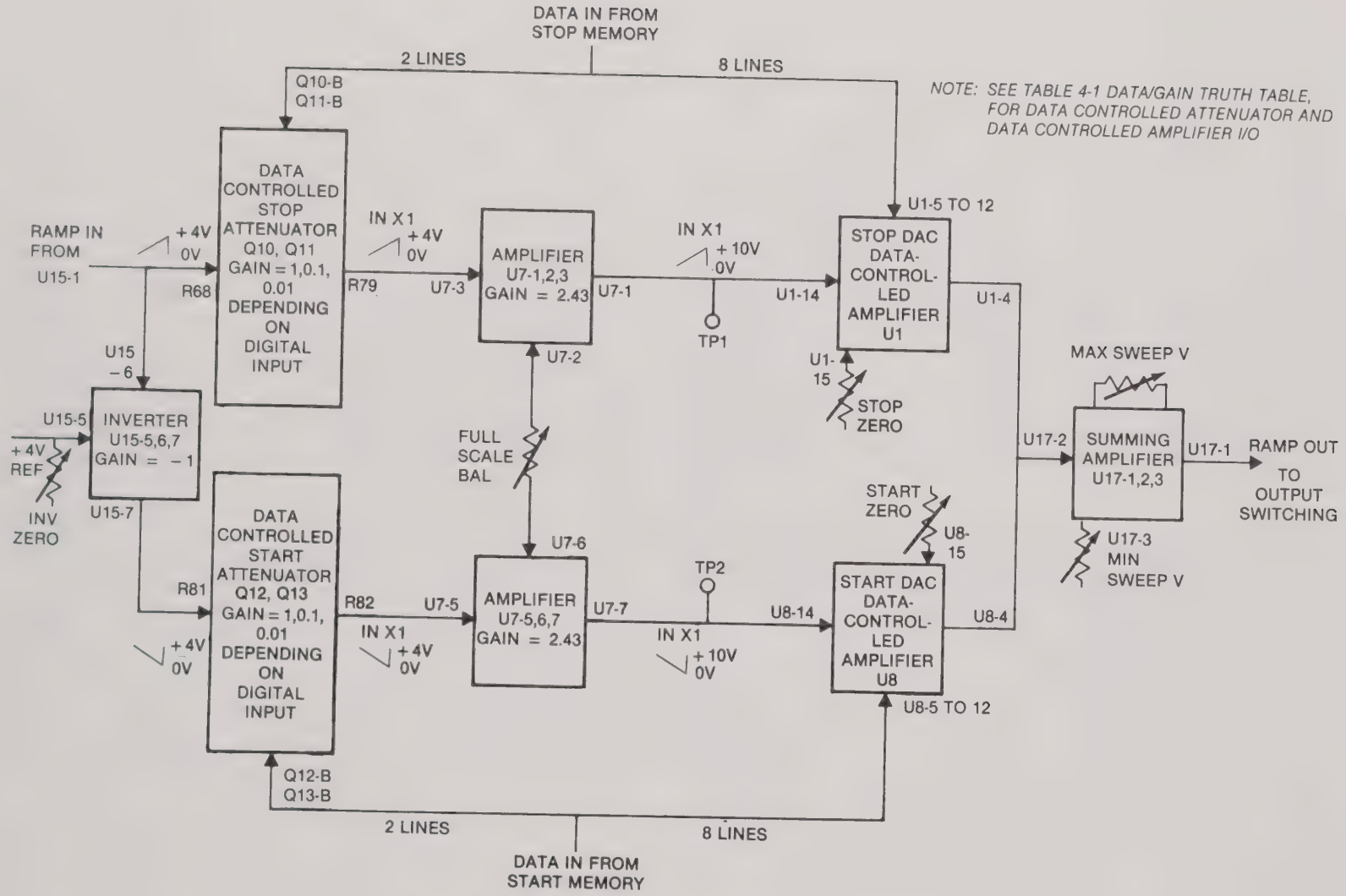


Figure 4-7. Three-Decade Multyiplying DAC Block Diagram

3) Set +4V line is activated so the 0 to +4 volt reference ramp is forced to +4 volts, the end of sweep voltage. This stops the sweeping of the reference ramp, and coordinates the reference to the proper VCG value. Since the reference ramp is forced to +4 volts, the voltage to the input of the start DAC is 0 (because of inversion).

Phase 2 is approximately 80 ms later, and is the process that sets the memories. The three steps of phase 2 are:

1) The reset is removed from both the stop 2 bit and 8 bit memories.

2) The stop memory clock (U26 pins 4, 5, 6, 8, 9, 10) is enabled causing the stop DAC memory to count up. As the memory counts up the output of the stop DAC starts to increase. In this mode, the stop DAC is being used as a digital to analog converter while the memory is being used as a counter. Since the start DAC is reset at 0 its output remains at zero.

3) When the stop memory contains the byte 1111 1110 the nand gate U3 goes low. The VCG produced by the stop DAC is +4 volts for all practical purposes, and phase 3 begins.

Phase 3 sets the memories. The 2 steps of phase 3 are:

1) Stop the clock so the byte content of 1111 1110 is retained in the stop memory. This is the setting used for full sweep.

2) Remove the Set +4V, which allows the reference ramp to run again.

Phase 4 (fixed approximately 130 ms). This phase is used to "clean house". Upon completion of phase 4, the circuit is prepared to receive any new settings to be initiated or is set for a continuous running mode. Refer to table 4-1 to confirm the data/gain logic levels for full sweep.

NOTE

For detailed full sweep description, refer to Appendix A.

In selecting SET START or SET STOP the user desires to begin at a certain frequency and end at another. Hence a VCG signal generated by the summing ramp principle is needed. Like full sweep, to set the start memory and the stop memory requires four phases of action. The process is not exactly like full sweep; so to illustrate the action, assume a hypothetical sweep that starts at 1.5 kHz (and stops at 3.5 kHz). Assume the sweep is on, thus the dial is out of the VCG circuit (see figure 4-2), the sweep is sweeping, and the main generator is set in the 1K range. The four set start phases are as follows.

Phase 1 is initiated by pressing SET START button. The four steps of this phase are:

1) The dial voltage is switched into the VCG circuit and the sweep ramp is switched out. Thus the dial at this instant controls the main generator's frequency.

2) The 2 bit start memory is set to binary 11. This causes maximum attenuation for the inverted reference ramp to the start DAC.

3) The 8 bit start memory is reset to 0. This causes the start DAC to have 0 gain.

4) SET 0V line is activated, which forces the reference ramp to 0 volts in set start. This input to the stop DAC causes the output to be 0 regardless of the stop DAC's memory setting and causes +4V (because of inversion) to be applied to the start DAC.

Phase 2 begins when the set start is released. The 4 steps of this phase are:

1) The dial voltge is switched out of the generator circuit and the sweep ramp is switched in.

2) The set state on the 2 bit attenuator is removed. This allows the attenuator of the start memory to be advanced to the right decade (as will be described in step 4).

3) The reset on the 8 bit memory is removed. This allows the start DAC memory to be advanced as will be described in step 4.

4) The start clock oscillator runs, advancing the start memory. As the memory advances, the DAC's gain increases. The resulting voltage output of U17 pin 1 is constantly being compared with the buffered dial at U18 pins 1, 2, 3. If by 255 counts the start DAC's output doesn't equal the desired dial buffer voltage, the most significant bit of the start memory U2 pin 6 advances the start attenuator memory U10 pin 9 to 0. This

Table 4-1. Data/Gain Truth Table

Two-Bit Start Attenuator

DATA INPUT U11-9 (Q13)	DATA INPUT U11-5 (Q12)	GAIN	COMMENTS
HI	HI	×0.01	ANY OF THESE STATES ARE POSSIBLE FOR "FULL SWP" CONDITION
LO	HI	×0.1	
LO	LO	1	
HI	LO		ILLEGAL STATE. TROUBLESHOOT U11, Q12, Q13 CIRCUITS

Two-Bit Stop Attenuator

DATA INPUT U10-9 (Q11)	DATA INPUT U10-5 (Q10)	GAIN	COMMENTS
HI	HI	×0.01	
LO	HI	×0.1	"FULL SWP" CONDITION
LO	LO	×1	
HI	LO		ILLEGAL STATE. TROUBLESHOOT U10, Q10, Q11 CIRCUITS

Eight-Bit Start/Stop Memories

DATA INPUT U1/U8 PIN (MSB) 5	6	7	8	9	10	11	(LSB) 12	RELATIVE GAIN OF U1/U8	COMMENTS
LO	LO	LO	LO	LO	LO	LO	LO	0	U8, (START DAC) "FULL SWP" CONDITION
LO ⋮ HI	LO ⋮ HI	LO ⋮ HI	LO ⋮ HI	LO ⋮ HI	LO ⋮ HI	LO ⋮ HI	HI ⋮ LO	VERY LOW ⋮ VERY HIGH	U1, (STOP DAC) "FULL SWP" CONDITION
HI	HI	HI	HI	HI	HI	HI	HI	MAX	

causes the start to be divided by 10. The counting continues. If the voltage isn't found in the second decade, the attenuator is advanced to divide by 1. Since the assumed frequency would require approximately 1.5 volts for a start VCG the third decade will give the correct attenuation. This is because the assumed value is above .4 on the dial. Thus when the attenuator is set to divide by 1, the DAC counts up until a match is made in this decade. Phase 3 now begins.

Phase 3 (DAC output equals dial voltage).

1) The start clock is disabled.
2) The SET 0V line is removed in set start mode.

The reference ramp is now free to continue.

Phase 4 is "house cleaning" in nature. As in full sweep, this prepares the circuit for continuous run and/or any new commands initiated. Refer to table 4-1 for data/gain truth table.

NOTE

For a detailed set start description, refer to appendix C.

Set stop is very similar to set start. As stated earlier, the example is a 1.5 kHz to 3.5 kHz sweep. Assume the sweep is on, thus the dial is out of the VCG circuit (see figure 4-2), the sweep is sweeping, and the main generator is set in the ×1K range. The following four phases occur in setting sweep stop to 3.5 kHz.

Phase 1 is initiated by pressing SET STOP button. The four steps of this phase are:

1) The dial voltage is switched into the VCG circuit and sweep ramp is switched out. Thus the dial at this instant controls the main generator's frequency.
2) The 2 bit stop memory is set to binary 11. This causes maximum attenuation for the non-inverted reference ramp to the stop DAC.
3) The 8 bit stop memory is reset to 0. This causes the stop DAC to have 0 gain.
4) SET +4V line is activated, which forces the reference ramp to +4 volts. This input to the start DAC is inverted to 0 and forces the output to be 0 regardless of the start DAC's memory setting and causes a +4 voltage to be applied to the stop DAC.

Phase 2 begins when the set stop is released. The 4 steps of this phase are:

1) The dial voltage is switched out of the generator circuit and the sweep ramp is switched in.
2) The set state on the 2 bit attenuator is removed. This allows the attanuator of the stop memory to be advanced to the right decade (as will be described in step 4).
3) The reset on the 8 bit memory is removed. This allows the stop DAC memory to be advanced as will be described in step 4.
4) The stop clock oscillator runs, advancing the stop memory. As the memory advances, the DAC's gain increases. The resulting voltage output of U17 pin 1 is constantly being compared with the buffered dial at U18 pins 1, 2, 3. If by 255 counts the stop DAC's output doesn't equal the desired dial buffer voltage, the most significant bit of the stop attenuator memory U9 pin 8 advances the stop attenuator memory U10 pin 9 to 0). This causes the stop to be divided by 10. The counting continues. If the voltage isn't found in the second decade, the attenuator is advanced to divide by 1. Since the assumed frequency would require approximately 3.5 volts for a stop VCG, the third decade will give the correct attenuation. This is because the assumed value is above .4 on the dial. Thus when the attenuator is set to divide by 1, the DAC counts up until a match is made in this decade. Phase 3 now begins.

Phase 3 (DAC output equals dial voltage).

1) The stop clock is disabled.
2) The SET +4V line is removed in set stop mode.

The reference ramp is now free to continue.

Phase 4 is "house cleaning" in nature. As in full sweep and set start, this prepares the circuit for continuous run and/or any new commands initiated. Refer to table 4-1 for data/gain truth table.

NOTE

For a detailed set stop description, refer to appendix B.

Some final notes on the sweep board. The ramping at TP1 and TP2 are the reference ramp after it has been attenuated and amplified to compensate for the decrease in DAC unity gain. Hence, TP1 will sweep from 0 to 9.6 volts (in the third decade of attenuation) and TP2 will sweep 9.6 to 0 volts (in the third decade of attenuation). TP3 is on the VCG line of the main generator.

Refer to figures 4-8 and 4-9 for a block diagram clarification of the rear panel outputs, dial buffer output switching, and sweep indicator circuits.

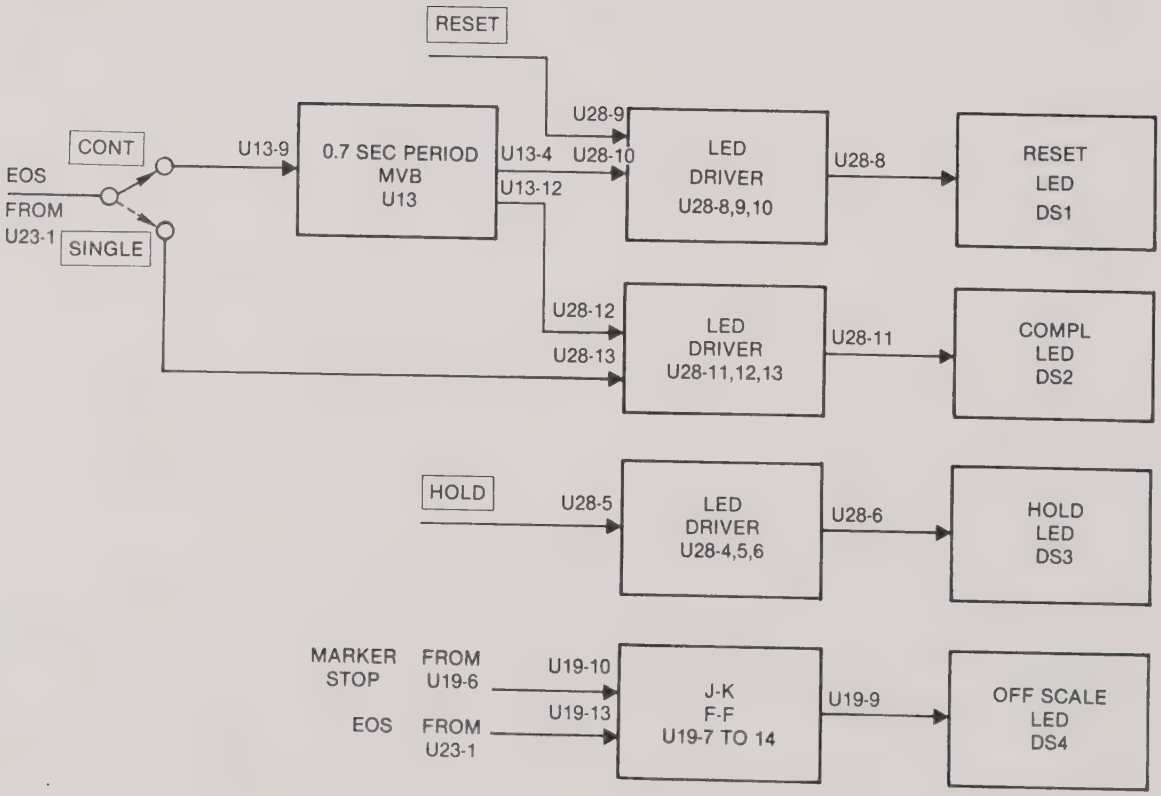


Figure 4-8. Sweep Indicator Circuits

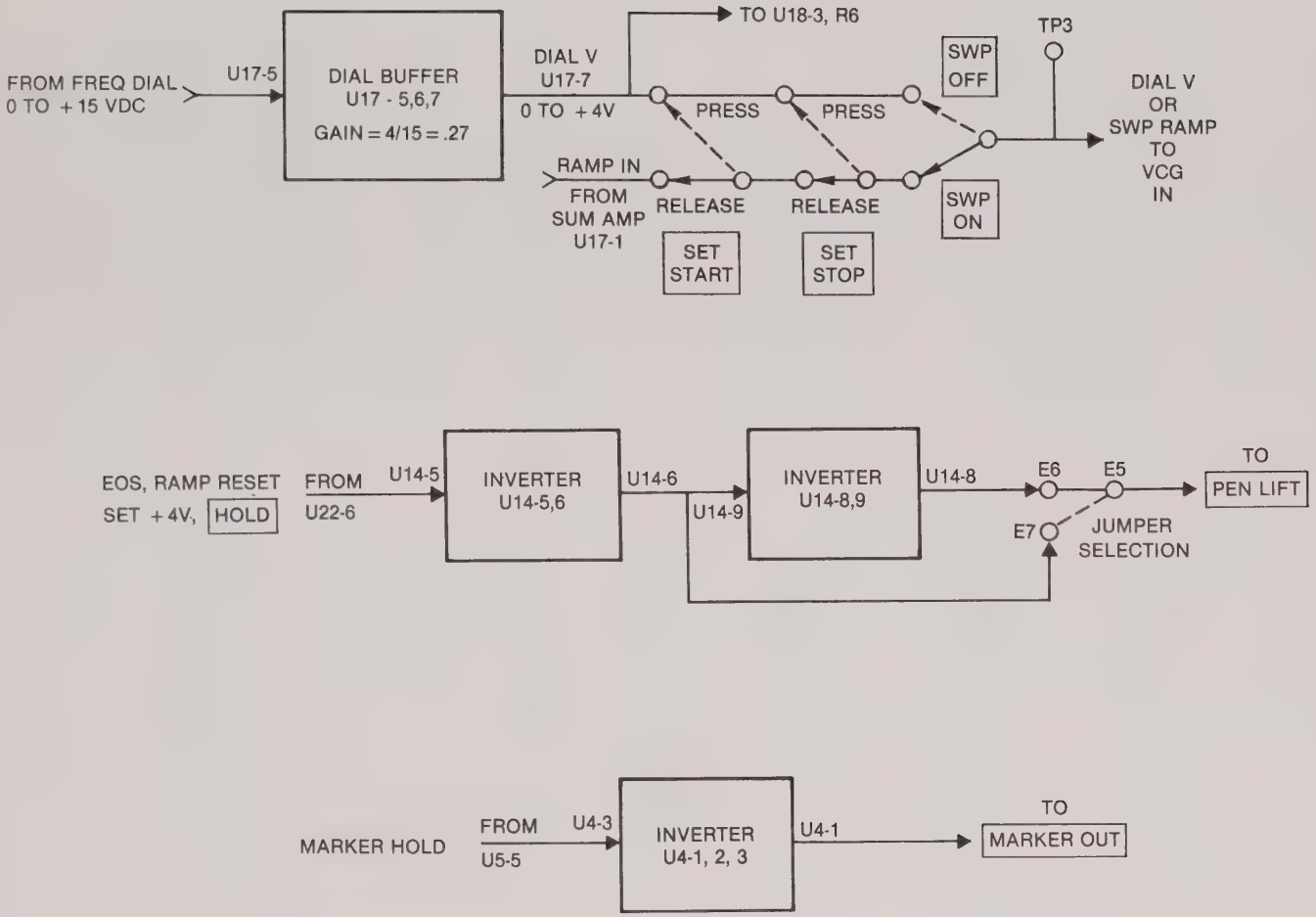


Figure 4-9. 189 Sweep Dial Buffer/Output Switching and Rear Panel Outputs

SECTION 5
ALIGNMENT

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for alignment or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter . . Millivolt dc measurement (1% accuracy)
Oscilloscope . . . . . ≥60 MHz bandwidth
Counter . . . . . 4 MHz (0.1% accuracy)
50Ω Feedthru . . . . . ±1% accuracy, 2W
Distortion Analyzer . . . . . To 400 kHz
RG58U Coax Cable . . . 3 ft length BNC male contacts

5.3 REMOVING GENERATOR COVERS

1. Invert the instrument and remove the four screws in the bottom cover (ref: drawing 0102-00-0869 in section 7).

2. Turn the instrument upright, remove the top cover for access to generator board alignment controls.

3. For access to the sweep board, remove the screws securing the bottom cover to the generator board, replace the top cover, invert the instrument and remove the bottom cover.

4. When alignment is complete, secure the top and bottom cover with screws.

NOTE

Remove the cover only when it is necessary to make adjustments or measurements.

5.4 ALIGNMENT

After referring to the following preliminary data, perform alignment, as necessary, per table 5-1. If performing partial alignment, check previous settings and adjustments for applicability.

1. All measurements made at the FUNCTION OUT connector must be terminated into a 50Ω (±1%) load.

2. Start the alignment by connecting the unit to an appropriate ac power source and setting the front panel switches as follows.

FREQUENCY DIAL 4.0
FREQUENCY MULTIPLIER 1K
MODE . . . . . CONT
FUNCTION . . . . . ⊓
DC OFFSET . . . . . OFF
AMPLITUDE . . . . . MAX
LOG/LIN . . . . . LIN
SWEEP ON/OFF . . . . . OFF
MARKER . . . . . OFF

3. Allow the unit to warm up at least 30 minutes for final alignment. Keep the instrument cover on to maintain heat. Remove cover only to make adjustments or measurements.

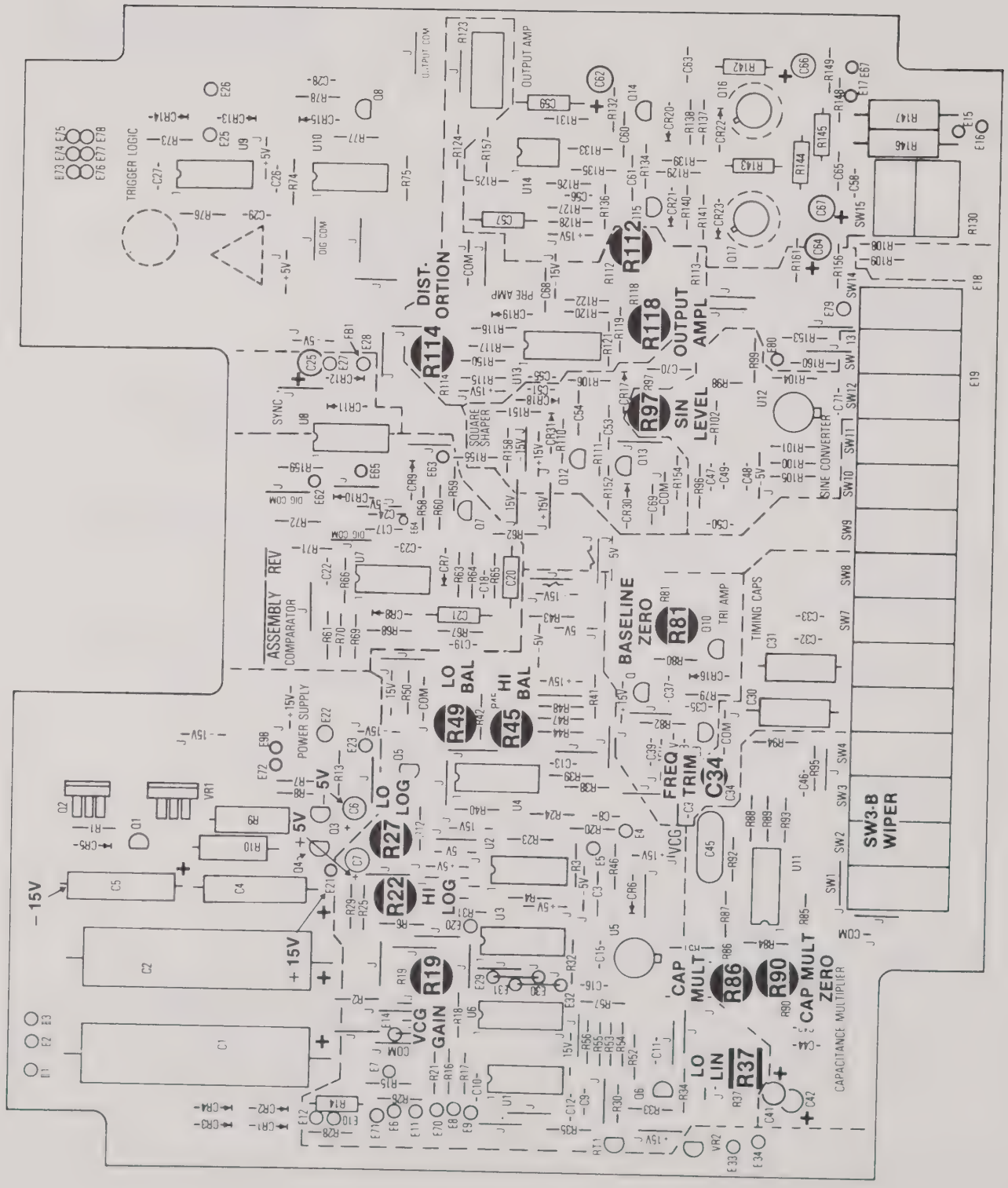


Figure 5-1. Generator Board Alignment Points

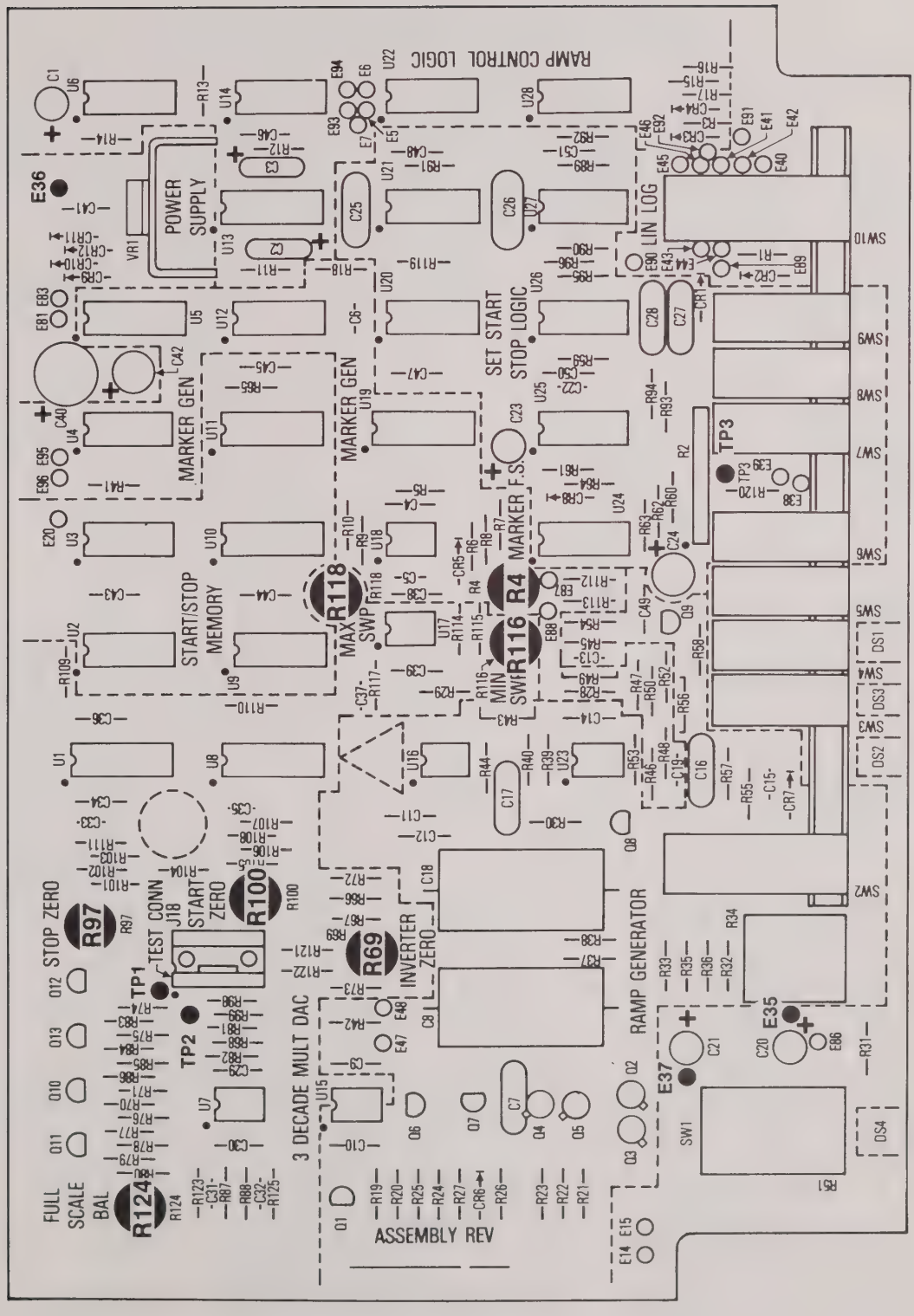


Figure 5-2. Sweep Board Alignment Points

Table 5-1. Alignment Procedure

Note: Open column indicates previous entry remains applicable.

Step	Check	Tester	Test Point	Control Setting	Adjust	Results	Remarks
1	Mechanical Dial Alignment	If dial or pot have been removed or replaced, calibrate by removing dial and rotate pot shaft fully clockwise against stop. Slide the dial on the shaft and rotate dial fully clockwise against the dial stop. Adjust dial axially so that the dial stop projects ½ depth of indicator. Tighten dial set screw.					
2	Power Supply	Voltmeter	C4 +	Paragraph 5.4, Step 2		+ 15 ± .75V	Verify. ± 15V should track within 30 mV.
3			C5 –			– 15 ± .75V	
4			C7 +			+ 5 ± .25V	Verify.
5			C6 –			– 5 ± .25V	
6	Capacitor Multiplier Zero		SW3 - B Wiper		R90 CAP MULT ZERO	0 ± 2 mV	
7	Approximate Bottom of the Dial Frequency	Counter	50Ω OUT HI (terminate into 50Ω	Dial: .004 FREQ MULT: 10K	R37 LO LIN	20 to 25 ms period	
8	Bottom of the Dial Symmetry	Scope			R49 LO BAL	Equalize (+) and (–) half cycles	Set scope to (–) trigger; display one full cycle. Align positive transition to center of screen. Multiply the horizontal display × 10. Set scope to (+) trigger; adjust R49 to align negative transition with center of screen.
9	Bottom of the Dial Frequency (Lin)	Counter		FREQ MULT: × 1K	R37 LO LIN	350 ± 50 ms period	
10	Top of the Dial Symmetry	Scope		Dial: 4.0	R45 HI BAL	Equalize (+) and (–) half cycles	See step 8.
11	Top of the Dial Frequency (Lin)	Counter		Dial: 4.0 FREQ MULT: × 1K	R19 VCG GAIN	4 (± .02) kHz	
12				FREQ MULT: × 10K		40 (± .8) kHz	Verify.
13				FREQ MULT: + 1M	C34 FREQ TRIM	4 (± .02) MHz	
14				FREQ MULT: × 100K		400 (± 8) kHz	Verify. If necessary, trim by changing value of C33.

Table 5-1. Alignment Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Results	Remarks
15				FREQ MULT: ×100	R86 CAP MULT	2.5 (±.05) ms	
16				FREQ MULT: ×10		25 (±.5) ms	Verify.
17				FREQ: ×1		250 (±5) ms	
18	Bottom of the Dial Frequency (Log)			Dial: .0004 FREQ MULT: ×100K	R27 LO LOG	40 ±2 Hz	Allow 1 hour warm-up before checking.
19	Top of the Dial Frequency (Log)			Dial: 4.0 FREQ MULT: ×100K	R22 HI LOG	400 kHz ±10 kHz	Repeat steps 18 and 19 once.
20	Sine Distortion (Lin)	Distortion Analyzer		FUNCTION: ∿ FREQ MULT: ×1K	R97 SINE LEVEL R114 DISTOR-TION	Adjust for minimum distortion	It may be necessary to reduce amplitude to 5V peak.
21	Output Amplitude	Scope		FUNCTION: ∿	R118 OUTPUT AMPL	10 Vp-p (+.3V/−0V)	
22	Output Offset	Voltmeter		FUNCTION: ∿	R112 OFFSET	0 (±50) mV	
23	Baseline Zero	Scope		MODE: Trigger	R81 BASE LINE	0 (±75) mV	It may be necessary to trim the baseline with R80.

The following steps are performed on the sweep board.

24	Power Supply	Voltmeter	E36			+5 ±.25V	Verify.
25			E35			+15 ±.75V	
26			E37			−15 ±.75V	
27	End of Sweep Reset Pulse Time		Pen Lift (Unterminated)	SWEEP: ON SWP TIME: FAST		≥6 μs to ≤12 μs	
28				SWP TIME: SLOW		≥600 μs to ≤1200 μs	
29	Sweep Ramp	Scope	SWP OUT (Unterminated)			0 to 4V ramp	
30	Sweep Time		SWP OUT (Unterminated)	SWEEP TIME: FAST		≤100 μs to ≥0.6s	

Table 5-1. Alignment Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Results	Remarks
31				SWEEP TIME: SLOW		≤20 ms to ≥120s	
32	Sweep Logic	Scope and Front Panel Annunciators		SWEEP: ON SWEEP TIME: SLOW MARKER: OFF HOLD: In		Hold Annunciator Lights. Ramp Stops at dc level.	
33				HOLD: Out SINGLE: In		Compl Annunciator Lights. Ramp Stops at +4V.	
34				RESET: In		RST Annunciator Lights. Ramp Stops at 0V	
35	Set Start Ramp Voltage	Voltmeter	SWP OUT (Unterminated)	SET START: Press and hold		0V ±0.025V	Verify. Hold SET STOP in while making reading.
36	Set Stop Ramp Voltage			SET STOP: Press and hold		4 ±0.25V	Verify. Hold SET START in while making reading.
37	Inverter Zero	Voltmeter. Optional: Insert 5 position DIP switch or test fixture into J18. All positions are open. Be sure DIP switch 1 is aligned with pins 1 and 14 of J18.)	TP-2	SINGLE: In RESET: Out FULL SWEEP: Press Test Connector J18: Momentarily short pins 5 and 10. (DIP SWITCH: Momentarily close sw 5.)	R69 INV ZERO	0 ±0.004V	
38			TP-1			9.6 ±0.5V	Verify.
39	Inverter Scaling		TP-2	SINGLE: Out RESET: In		9.6 ±0.5V	
40			TP-1			0 ±0.04V	
41	Dial Buffer		TP-3	SWEEP: OFF Dial: .004		+0.005V ±0.010V	Verify. Record reading.
42	Minimum Sweep Voltage			J18: Short pins 2 to 13 and 4 to 11. (DIP sw: Close sw 2 and 4.) SWEEP: ON	R116 MIN SWP	Results from Step 41 minus 0.002V	Record Results.

Table 5-1. Alignment Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Results	Remarks
43	DAC Scale			J18: Open pins 2 to 13 and short pins 1 to 13 (DIP sw: Open sw 2 and close sw 1.) RESET: In	R97 STOP ZERO	Results from Step 42 plus 0.001V	Record Results.
44				J18: Open pins 1 to 14 and 4 to 11. Close pins 2 to 13 and 3 to 12. (DIP sw: Open sw 1 and sw 4. Close sw 2 and sw 3.) SINGLE: In RESET: Out	R100 START ZERO	Results from Step 43 plus 0.001V	Reading at TP3 should equal results from 41.
45	Dial Full Scale			Dial: Maximum ccw SINGLE: Out RESET: Out SWEEP: Out		+4 ±0.16V	Verify. Record results.
46	DAC Full Scale			SWEEP: ON J18: Open pins 2 to 13, close pins 1 to 14. (DIP sw: Open sw 2, close sw 1.)	R118 MAX SWP V	Results from Step 45 plus 0.1V	
47	Full Scale Balance	Scope (connect with X1 probe)		SWEEP TIME: 2 to 5 ms	R124 FULL SCALE BALANCE	10 mV p-p maximum ac value	Disregard reset transient. Set scope to ac coupling, 10 mV/div in vertical and 1 ms/div in horizontal.
48	Marker Function	Scope with X-Y	Connect: SWP OUT to X input, (External horizontal) 50Ω OUT to Y input (vertical)	J18: Remove Jumpers, DIP sw, or test fixture SWEEP: ON FULL SWEEP: In MARKER: On SWEEP TIME: FAST Dial: Full cw FREQ MULT: ×1M FUNCTION: ∿		Marker appears on scope. Sweep envelope shows uniform rolloff.	Verify.
49				Dial: Rotate ccw		Marker moves as dial is rotated.	
50				MARKER DURATION: Rotate from ccw to cw.		Marker intensity increases as control is rotated.	

Table 5-1. Alignment Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Results	Remarks
51	Marker Scale			Dial: Set to 3.8 START: Press Dial: Set to 4.0 STOP: Press	R4 MARKER FULL SCALE	Set Marker 10% (1 div) from end of sweep.	
52	Marker Duration	SCOPE	SWP OUT (Unterminated)	MARKER DURATION: rotate from ccw to cw.		Marker duration varies from 2% to 60% of sweep time.	Verify.
53	Sweep Drift in Hold or Marker		50Ω OUT HI (terminate into 50Ω)	Dial: .6 (initial) FREQ MULT: 1K. FUNCTION: ⊓⊔ . SWP TIME: FAST and MAX. MARKER DURATION: MAX. FULL SWP: In		Drift less than ±1 div out of 8 in 5 sec.	Verify. Set scope to ±0.2 ms/div. Adjust MARKER FREQ dial to display 1 cycle in 8 divisions during marker. At next marker press SWEEP HOLD, and check for drift.

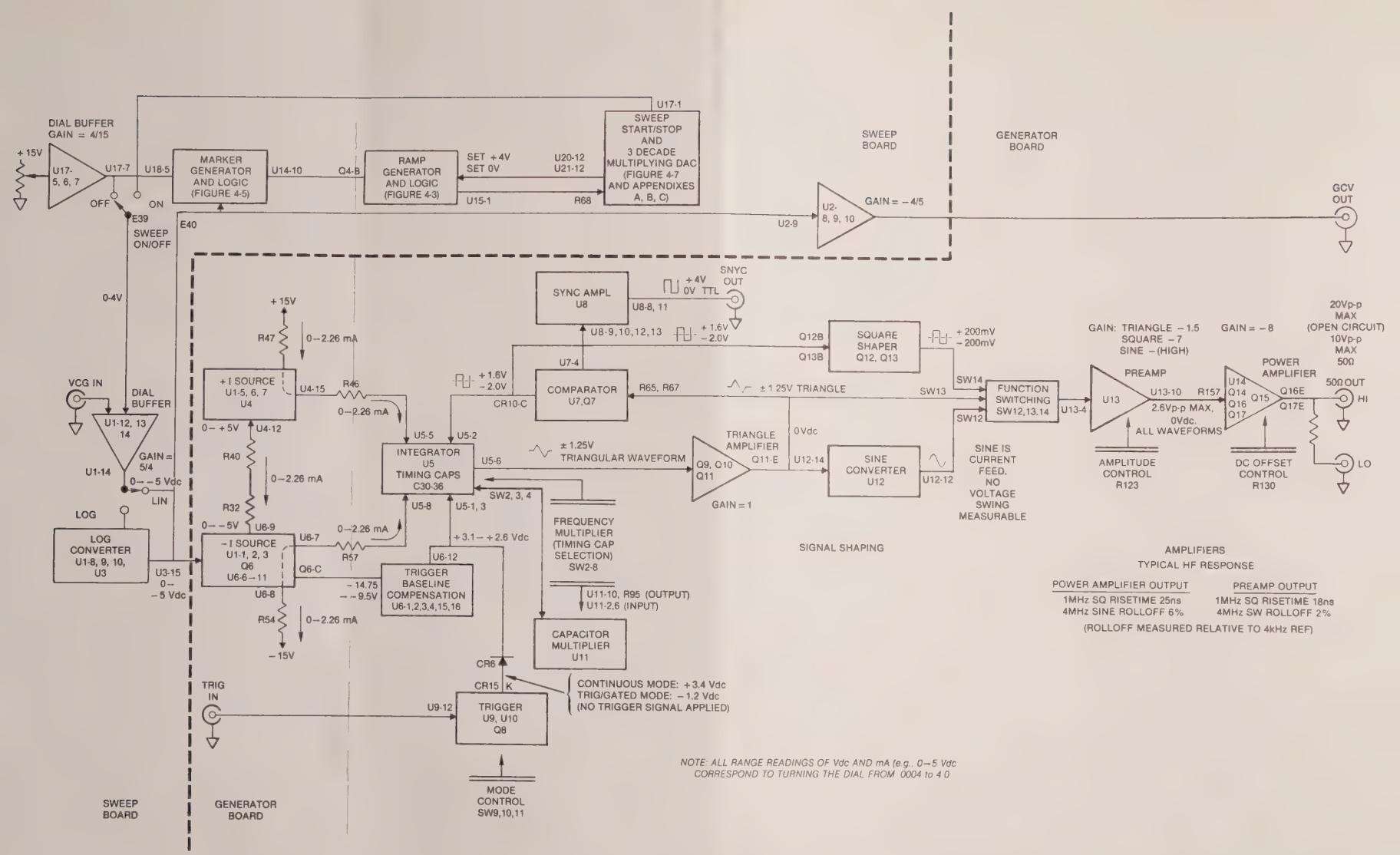


Figure 6-1. Generator Board Troubleshooting Block Diagram

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for alignment or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

CAUTION

To prevent damage to components, turn unit off while removing or replacing components, connectors or pc boards.

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which if applied consistently will lead to the problem area.

This troubleshooting guide is arranged to aid you in meeting the following goals.

1. Symptom recognition (listing of possible problem).
2. Symptom elaboration (front panel manipulation to isolate problems).
3. Isolation to the faulty function.
4. Isolation to the faulty circuit.
5. Isolation to the faulty component.

The functional blocks and their purpose are listed in table 6-1 as a supplement to figures 4-1 and 6-1. All information presented will revolve around this list. Figure 6-1 is the generator board portion of figure 4-1 annotated with troubleshooting data.

Table 6-1. Purpose of Each Circuit

Functional Block	Purpose
Power Supply	Supply regulated ±15 Vdc and ±5 Vdc to all circuits.
Dial Buffer	Buffer amplifier (voltage gain = −⅓). For isolation between the frequency dial pot and the following circuits.
−I Source	Constant current source (negative). The output level of which can be set from 0 to approximately 2.26 mA by the output of the dial buffer. The current output, applied to the integrator, results in the linear negative-going triangle slope. The −I source also outputs a second 0 to 2.26 mA to the +I source.
+I Source	Constant current source (positive). The output level of which can be set from 0 to approximately 2.26 mA by the output (U6-9) of the −I source. The current output, applied to the integrator, results in the linear positive-going triangle slope.

Table 6-1. Purpose of Each Circuit (continued)

Functional Block	Purpose
Integrator	Forms a linear triangular waveform as a result of alternate application of + and − charging current to a timing capacitor. Alternation is controlled by a square-wave signal applied from the comparator. This is accomplished through the use of a diode bridge, timing capacitors and appropriate range switching.
Triangle Buffer	Unity-gain FET-input noninverting buffer amplifier. Provides sufficient drive for the following circuits.
Comparator	Monitors the output of the triangle buffer and provides a control signal to the integrator that results in the generation of alternate positive- and negative- going linear ramps. The input of the comparator contains peak detection circuits that determine the ±1.25V peak levels of the resultant triangular waveform. The input circuits also contain R-C lead networks which "roll off" the triangle peaks during high frequency operation. The networks compensate for normal circuit delays, thus maintaining good dial tracking in the X100K and X1M frequency ranges. The control signal output to the integrator takes the form of a square wave which is also applied to trigger, sync and square shaper circuits.
Capacitor Multiplier	Used only in X1, X10 and X100 frequency multiplier ranges, this circuit shunts 90% (in X100), 99% (in X10) or 99.9% in (X1) of the current available from the ± I sources away from the timing capacitor, effectively "multiplying" the value of the timing capacitor by 10, 100 or 1000.
Sync Amplifier	Provides TTL level square wave (fan-out of 20) at the generator frequency to the front panel.
Trigger	Provides non-continuous generator operation by controlling application of the ± charging currents to the timing capacitor. In triggered mode, one cycle of waveform is generated each time the trigger input is driven to a TTL high level. In gated mode, the generator continues to run as long as the trigger input is held at a TTL high.
Trigger Baseline Compensation	Ensures that the output of the integrator remains at 0Vdc in triggered/gated operation with no trigger input.

Table 6-1. Purpose of Each Circuit (continued)

Functional Block	Purpose
Square Shaper	Conditions the square wave from the comparator to proper amplitude and waveshape by clipping the top and bottom of the waveform.
Sine Converter	Inputs triangular waveform and, through the use of nonlinear resistor-diode circuitry, outputs a sinusoidal current.
Preamp	Inputs selected waveform and amplifies it to 2.6 Vp-p for input to the power amplifier. Gain is −1.5 in triangle, −7 in square. It is current fed.
Power Amplifier	Complementary symmetry amplifier. Capable of delivering 10 Vp-p into 50Ω. Gain is −8 (open circuit) −4 (into 50Ω].
Ramp Generator and Control Logic	0 to −4V reference ramp for the sweep generator and sweep out BNC. Any condition forced onto this ramp is reflected in the sweeping of the main generator.
Marker Generator and Control Logic	Timed hold to the ramp generator.
Sweep Start/Stop and Control Logic	Adjusts and syncs the reference ramp to the proper start/stop level.

6.3 STARTING

When confronted with a problem, intially check the power supplies (figure 6-2). Once the power supplies are determined to be good, use the front panel manipulation to isolate the problem and refer to table

6-2, an index of the troubleshooting tables by indications of common problems. Table 6-2 and referenced figures do not cover every possible trouble, but, when used in conjunction with circuit descriptions and schematics, will be an aid in systematically isolating faulty components.

Once the problem is isolated to the smallest possible number of components, test individual components. Paragraph 6.4 suggests methods of testing many of the commonly used components.

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transitor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.

2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.

3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500mV forward voltage (or reversed bias), the transitor is defective.

4. A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).

5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

Table 6-2. Fault Isolation

Note: Return as many of the front panel controls as possible to their initial settings and still retain the problem. The troubleshooting tables generally begin at these initial settings and specify all subsequent setups. Preset the front panel controls as follows:

Control	Position
For Generator Board Troubleshooting	
Frequency Dial	4.0
POWER	ON
MODE	CONT
FREQ MULT	1 K
FUNCTION	
DC OFFSET	OFF
AMPLITUDE	MAX
SWEEP ON/OFF	OFF
For Sweep Board Troubleshooting	
SWEEP ON/OFF	ON
SNGL, RST, HOLD	OUT
TIME	CCW
MARKER	OFF

Problem	Figure
Power Supply	6-2
Symmetry or Frequency (Power Supplies OK)	6-3
Improper Amplitude or Waveshape of Any Function	6-5
No Output (Power Supplies OK)	6-6
Sweep Out Hung at 0V	6-7
Sweep Out Hung at ≈ +4V	6-8
Sweep Out Hung at > +4V	6-9
Sweep Out Hung Between 0 and +4V	6-10
No Marker	6-11
Marker Drifts Excessively	6-12
Full Sweep Logic Problems	6-13
Set Stop Logic Problems	6-14
Set Start Logic Problems	6-15

6.4.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.4.3 Operational Amplifier

1. The "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" inpout (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.
3. If the device supplying gate voltage to an FET saturates, the FET has too large a Vgs (pinch off) for the circuit and should be replaced.

6.4.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.4.6 Digital TTL IC's (e.g. 7400 Series)

1. The device is operating correctly if the output high state is > +2.4V and low state is < +0.5V.
2. The input must show the same two levels as in step 1. If the levels are between +0.8V and +2.0V, the connection to the driving circuit output is open.

6.5 INSTRUCTIONS FOR USING APPENDIXES

Each appendix shows a timing and sequence diagram. The relation between the timing and sequence diagram is as follows: At specified moments on the timing diagram there will be a sequence of events. These specified moments are labeled left to right on the sequence diagram. For example, in Appendix A the timing diagram is labeled SET, CLEAR, SET +80ms, MEMORY BYTE = 1111 1110 and CLEAR +130ms. Notice that the sequence diagram has sequence columns for four of the five specified moments.

Each sequence column then shows the order of cause and effect. Event 1 triggers event 2, event 2 triggers event 3 and so forth. Where an event may trigger more than one event, letters are used to designate another parallel sequence of events. For example event 2 triggers event 3 and event 3a. The continued string of events is designated by the same letter. Thus after 3a follows 4a.

When using these timing sequence diagrams, go to the last event of a column and note whether or not it occurs. if it does, go to the next column and check it. If the event doesn't occur troubleshoot those chips within the column. (See respective troubleshooting charts).

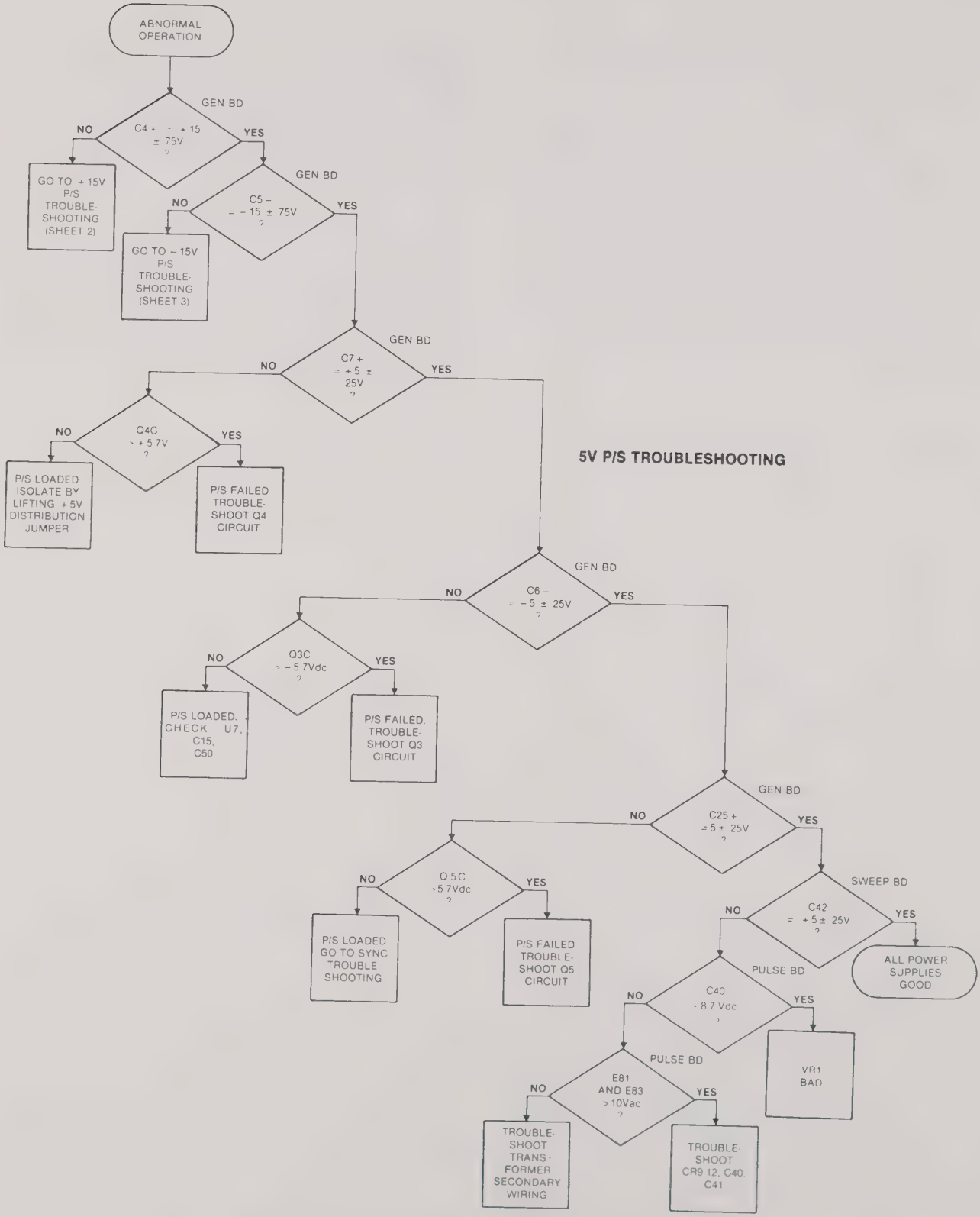


Figure 6-2. Power Supply Troubleshooting (Sheet 1)

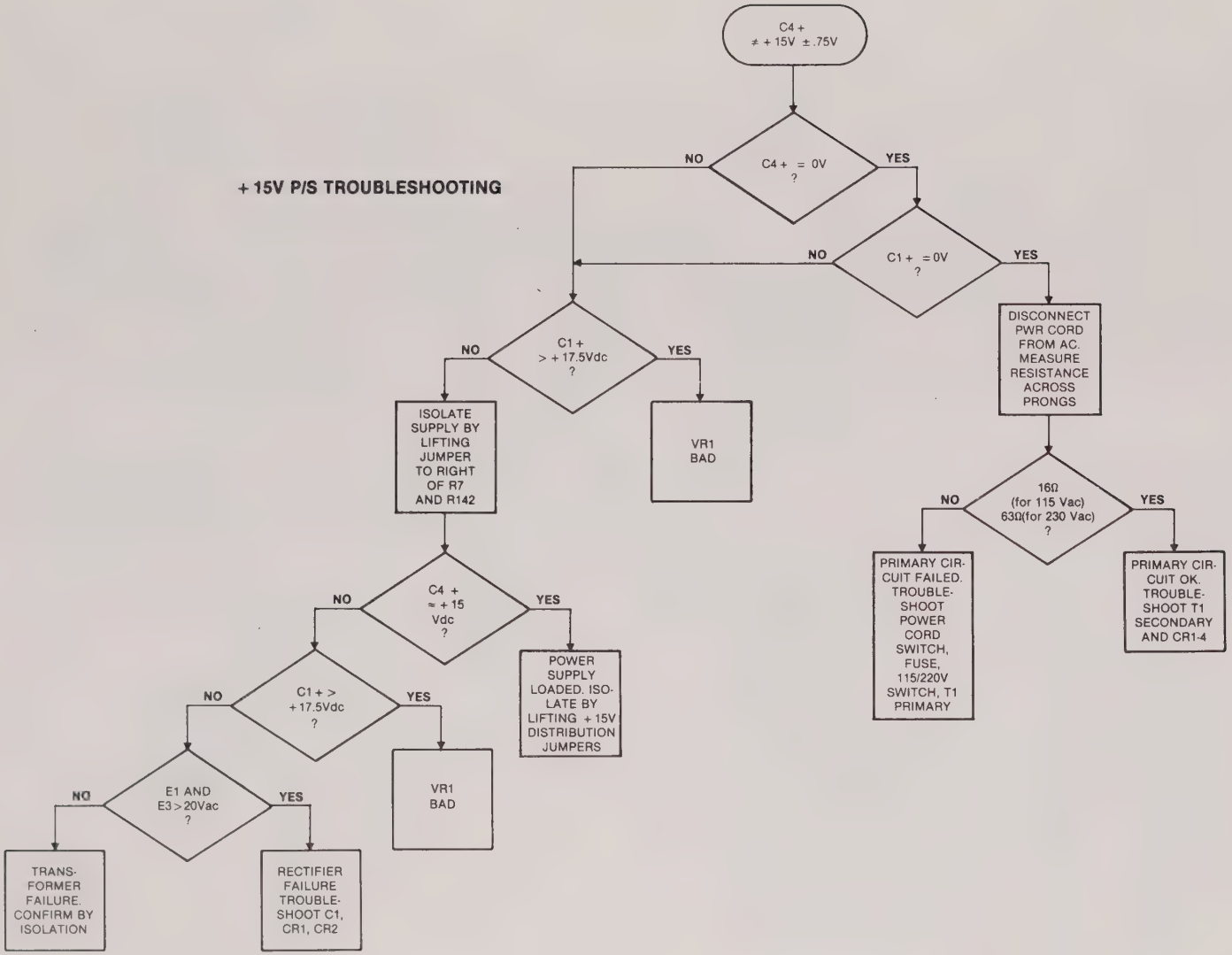


Figure 6-2. Power Supply Troubleshooting (Sheet 2)

– 15V P/S TROUBLESHOOTING

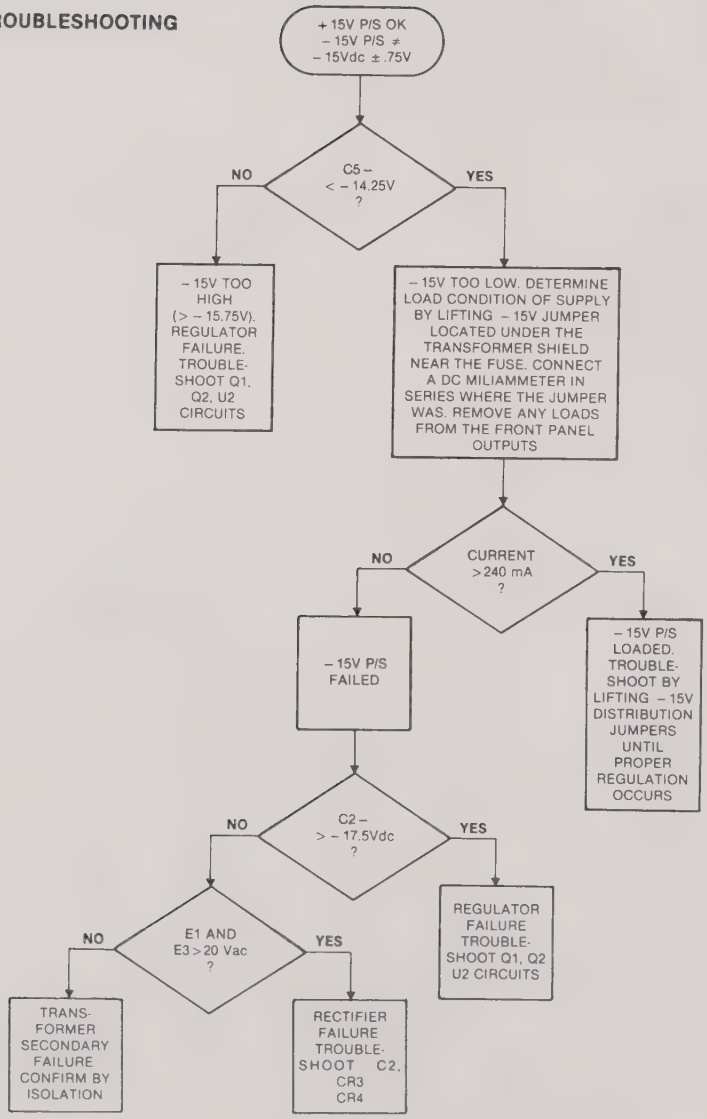

+ 15V P/S OK
– 15V P/S ≠
– 15Vdc ± .75V
C5 –
< – 14.25V
?
NO
YES
– 15V TOO HIGH (> – 15.75V). REGULATOR FAILURE. TROUBLE-SHOOT Q1, Q2, U2 CIRCUITS
– 15V TOO LOW. DETERMINE LOAD CONDITION OF SUPPLY BY LIFTING – 15V JUMPER LOCATED UNDER THE TRANSFORMER SHIELD NEAR THE FUSE. CONNECT A DC MILIAMMETER IN SERIES WHERE THE JUMPER WAS. REMOVE ANY LOADS FROM THE FRONT PANEL OUTPUTS
CURRENT
>240 mA
?
NO
YES
– 15V P/S FAILED
– 15V P/S LOADED. TROUBLE-SHOOT BY LIFTING – 15V DISTRIBUTION JUMPERS UNTIL PROPER REGULATION OCCURS
C2 –
> – 17.5Vdc
?
NO
YES
E1 AND E3 > 20 Vac
?
NO
YES
REGULATOR FAILURE TROUBLE-SHOOT Q1, Q2 U2 CIRCUITS
TRANS-FORMER SECONDARY FAILURE CONFIRM BY ISOLATION
RECTIFIER FAILURE TROUBLE-SHOOT C2, CR3 CR4

Figure 6-2. Power Supply Troubleshooting (Sheet 3)

NOTES ON BOTTOM-OF-DIAL (BOD) FAILURES

If BOD symmetry will not adjust, go to triangle mode and inspect linearity of the waveform.

Curvature of both sides of the triangle indicates a leak on line or in U5. Check BOD on X1K through X1M to check timing capacitors C30-C33. Measure voltage drop across R51: If any current is flowing, problem is in Q9, C34, C35, C36. If no current is flowing, problem is in U5.

A non-symmetrical triangle with or without curvature on one side only is an indication of failure in one current source or a leaky diode in U5. Determination of the failed circuit can be made by the following steps:

1. Measure voltage drop across R32 or R40. These drops should be equal and be in the 2 to 20 mV range.

2. Measure drops across R47 and R54. If either of these voltages is different from that measured in step 1, the problem lies in the circuit which shows the different voltage; that is, if the drop across R47 is different, problem is U4. If the voltage across R54 is different, the problem is U6. If all drops appear good, the problem is probably in U5. If changing U5 yields no improvement, the problem may still be a very small leak on the triangle generation line Q9, C34, C35, C36.

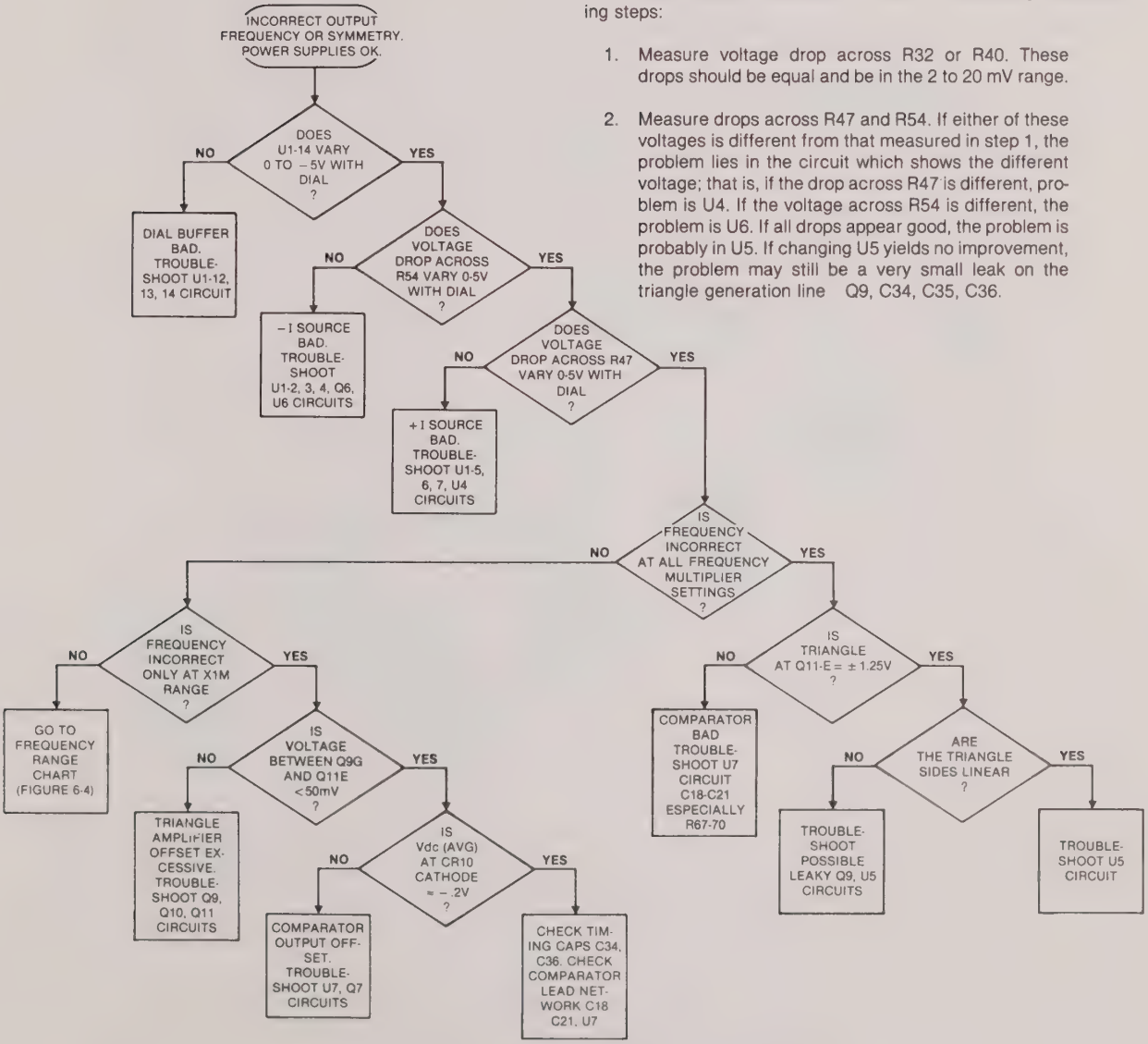

INCORRECT OUTPUT FREQUENCY OR SYMMETRY. POWER SUPPLIES OK.
DOES U1-14 VARY 0 TO −5V WITH DIAL ?
NO
YES
DIAL BUFFER BAD. TROUBLE-SHOOT U1-12, 13, 14 CIRCUIT
DOES VOLTAGE DROP ACROSS R54 VARY 0-5V WITH DIAL ?
NO
YES
−I SOURCE BAD. TROUBLE-SHOOT U1-2, 3, 4, Q6, U6 CIRCUITS
DOES VOLTAGE DROP ACROSS R47 VARY 0-5V WITH DIAL ?
NO
YES
+I SOURCE BAD. TROUBLE-SHOOT U1-5, 6, 7, U4 CIRCUITS
IS FREQUENCY INCORRECT AT ALL FREQUENCY MULTIPLIER SETTINGS ?
NO
YES
IS FREQUENCY INCORRECT ONLY AT X1M RANGE ?
NO
YES
GO TO FREQUENCY RANGE CHART (FIGURE 6-4)
IS VOLTAGE BETWEEN Q9G AND Q11E <50mV ?
NO
YES
TRIANGLE AMPLIFIER OFFSET EXCESSIVE. TROUBLE-SHOOT Q9, Q10, Q11 CIRCUITS
IS Vdc (AVG) AT CR10 CATHODE = −.2V ?
NO
YES
COMPARATOR OUTPUT OFFSET. TROUBLE-SHOOT U7, Q7 CIRCUITS
CHECK TIMING CAPS C34, C36. CHECK COMPARATOR LEAD NETWORK C18 C21, U7
IS TRIANGLE AT Q11-E = ±1.25V ?
NO
YES
COMPARATOR BAD TROUBLE-SHOOT U7 CIRCUIT C18-C21 ESPECIALLY R67-70
ARE THE TRIANGLE SIDES LINEAR ?
NO
YES
TROUBLE-SHOOT POSSIBLE LEAKY Q9, U5 CIRCUITS
TROUBLE-SHOOT U5 CIRCUIT

Figure 6-3. Symmetry or Frequency Problems

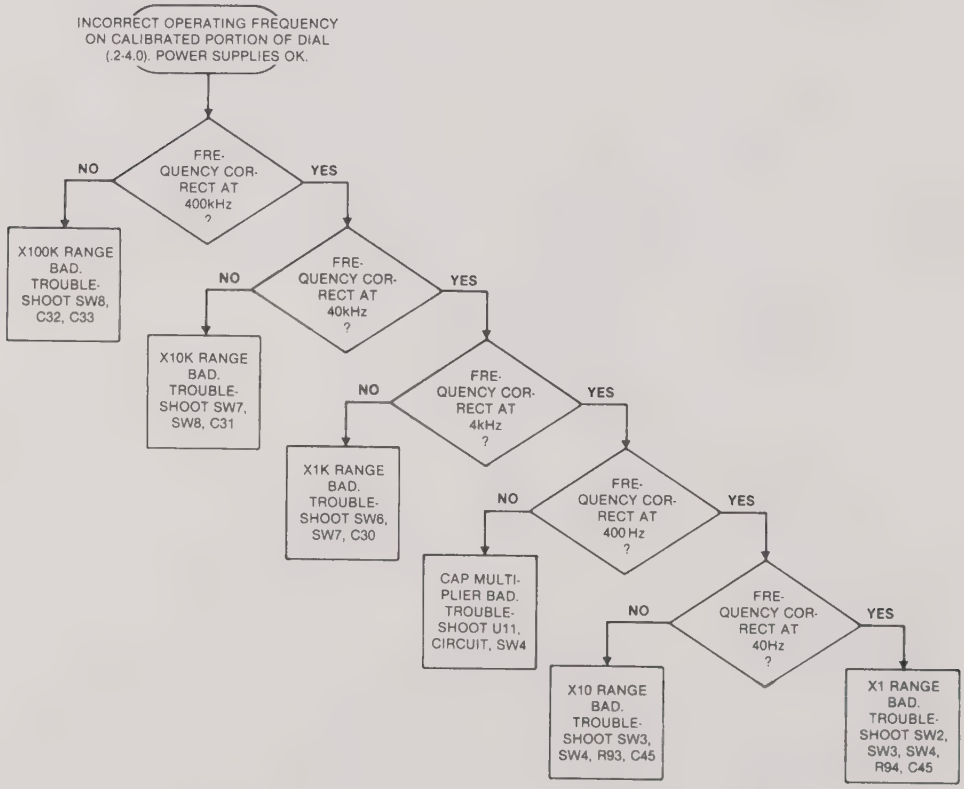

INCORRECT OPERATING FREQUENCY ON CALIBRATED PORTION OF DIAL (.2-4.0). POWER SUPPLIES OK.
FRE-QUENCY COR-RECT AT 400kHz ?
NO
YES
X100K RANGE BAD. TROUBLE-SHOOT SW8, C32, C33
FRE-QUENCY COR-RECT AT 40kHz ?
NO
YES
X10K RANGE BAD. TROUBLE-SHOOT SW7, SW8, C31
FRE-QUENCY COR-RECT AT 4kHz ?
NO
YES
X1K RANGE BAD. TROUBLE-SHOOT SW6, SW7, C30
FRE-QUENCY COR-RECT AT 400 Hz ?
NO
YES
CAP MULTI-PLIER BAD. TROUBLE-SHOOT U11, CIRCUIT, SW4
FRE-QUENCY COR-RECT AT 40Hz ?
NO
YES
X10 RANGE BAD. TROUBLE-SHOOT SW3, SW4, R93, C45
X1 RANGE BAD. TROUBLE-SHOOT SW2, SW3, SW4, R94, C45

Figure 6-4. Frequency Calibration Problems

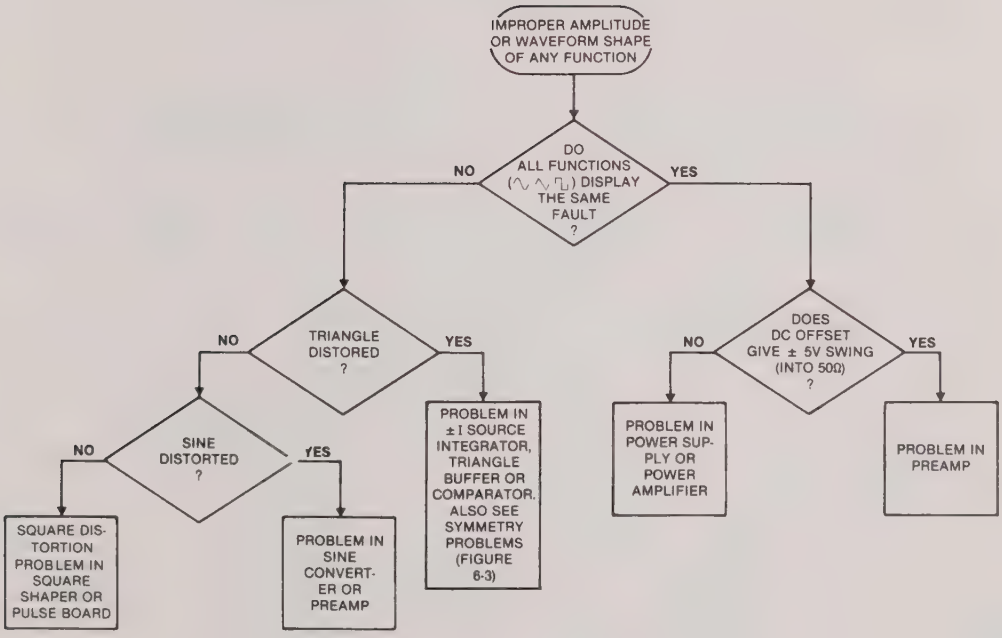

IMPROPER AMPLITUDE OR WAVEFORM SHAPE OF ANY FUNCTION
DO ALL FUNCTIONS (∿ ⋀ ⊓) DISPLAY THE SAME FAULT ?
NO
YES
TRIANGLE DISTORED ?
NO
YES
SINE DISTORTED ?
NO
YES
SQUARE DISTORTION PROBLEM IN SQUARE SHAPER OR PULSE BOARD
PROBLEM IN SINE CONVERTER OR PREAMP
PROBLEM IN ±I SOURCE INTEGRATOR, TRIANGLE BUFFER OR COMPARATOR. ALSO SEE SYMMETRY PROBLEMS (FIGURE 6-3)
DOES DC OFFSET GIVE ± 5V SWING (INTO 50Ω) ?
NO
YES
PROBLEM IN POWER SUPPLY OR POWER AMPLIFIER
PROBLEM IN PREAMP

Figure 6-5. Improper Amplitude or Waveshape

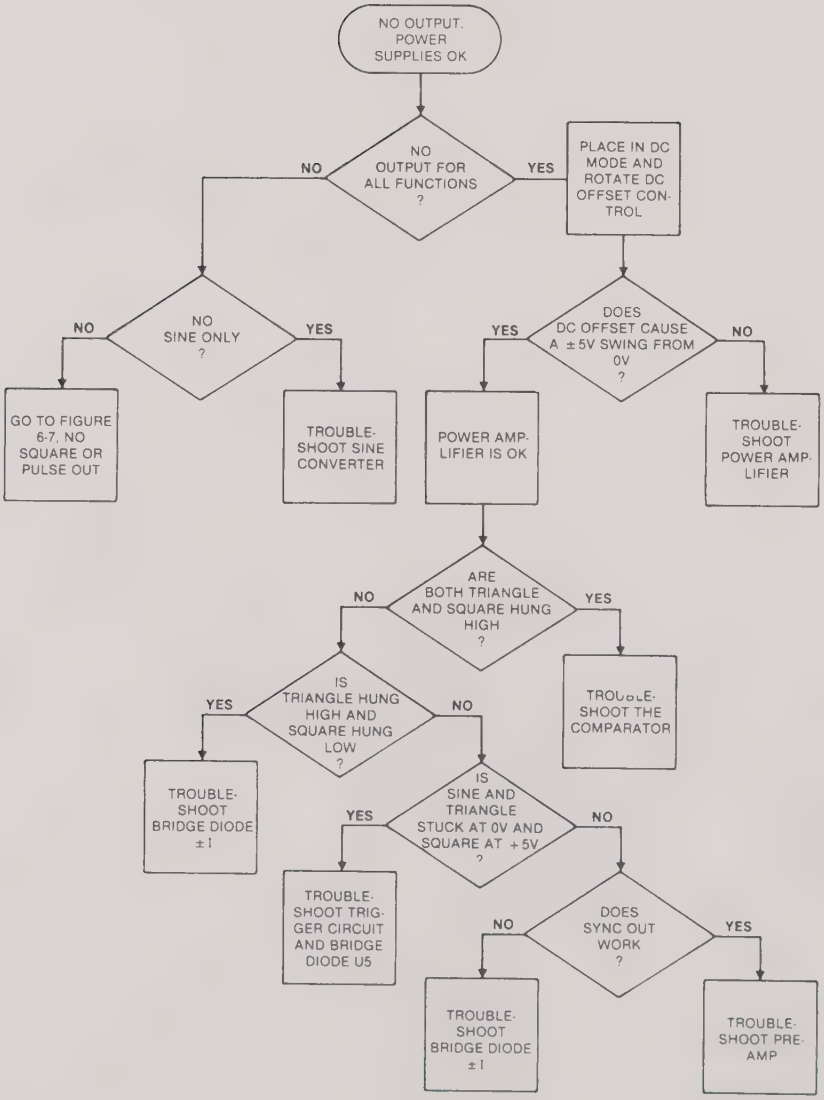


Figure 6-6. No Output

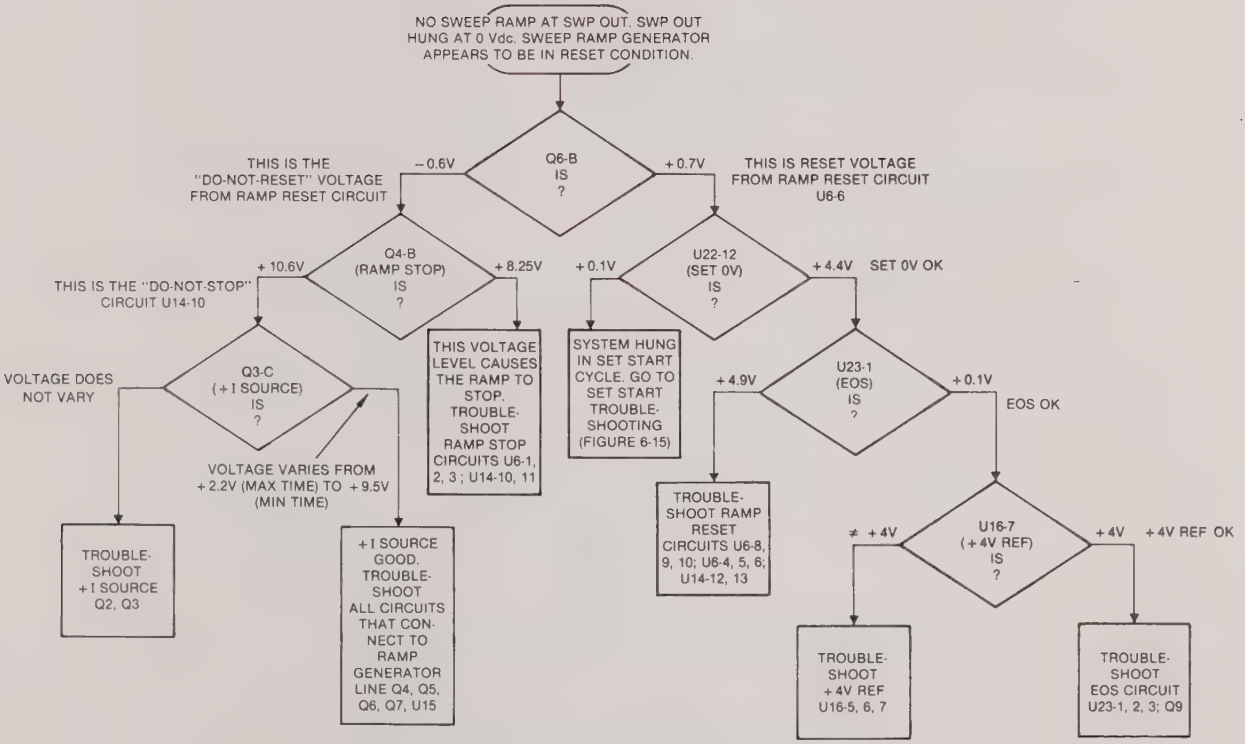
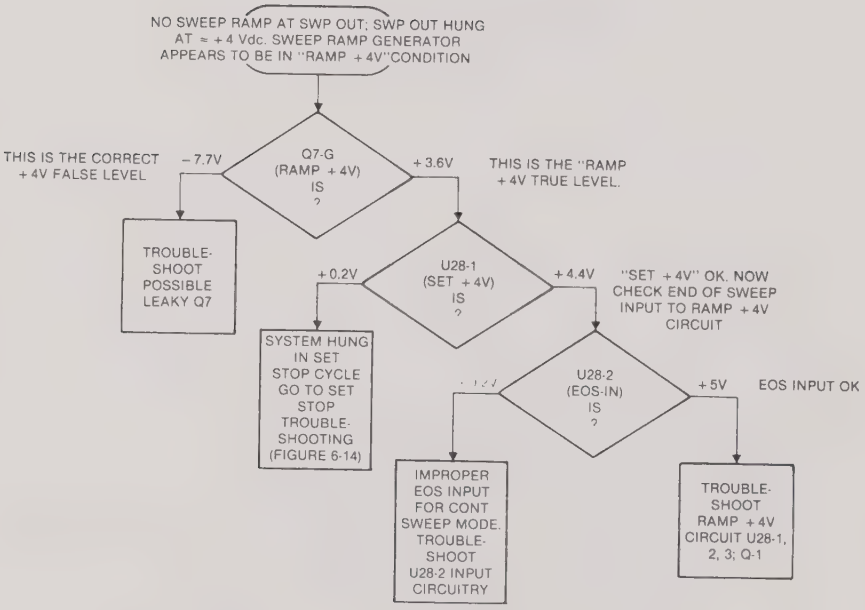
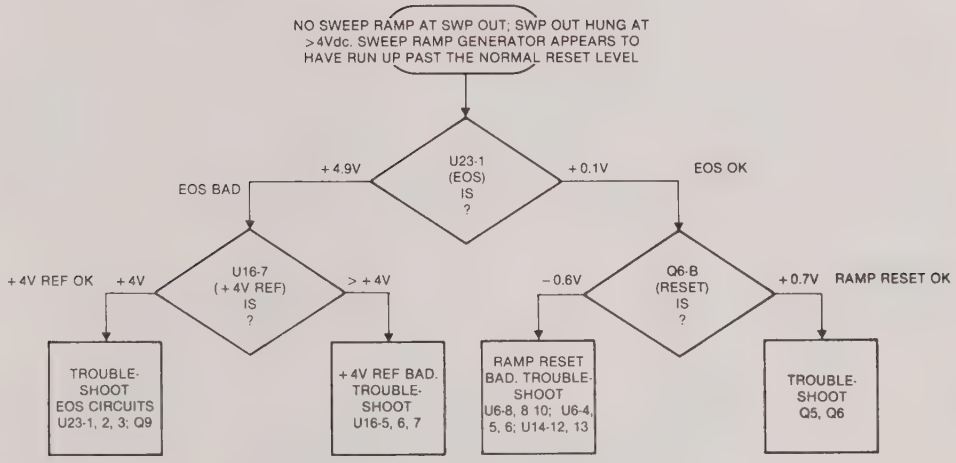

NO SWEEP RAMP AT SWP OUT. SWP OUT HUNG AT 0 Vdc. SWEEP RAMP GENERATOR APPEARS TO BE IN RESET CONDITION.
Q6-B IS ?
– 0.6V
THIS IS THE "DO-NOT-RESET" VOLTAGE FROM RAMP RESET CIRCUIT
+ 0.7V
THIS IS RESET VOLTAGE FROM RAMP RESET CIRCUIT U6-6
Q4-B (RAMP STOP) IS ?
+ 10.6V
THIS IS THE "DO-NOT-STOP" CIRCUIT U14-10
+ 8.25V
THIS VOLTAGE LEVEL CAUSES THE RAMP TO STOP. TROUBLE-SHOOT RAMP STOP CIRCUITS U6-1, 2, 3 ; U14-10, 11
U22-12 (SET 0V) IS ?
+ 0.1V
SYSTEM HUNG IN SET START CYCLE. GO TO SET START TROUBLE-SHOOTING (FIGURE 6-15)
+ 4.4V
SET 0V OK
Q3-C (+ I SOURCE) IS ?
VOLTAGE DOES NOT VARY
VOLTAGE VARIES FROM + 2.2V (MAX TIME) TO + 9.5V (MIN TIME)
TROUBLE-SHOOT + I SOURCE Q2, Q3
+ I SOURCE GOOD. TROUBLE-SHOOT ALL CIRCUITS THAT CONNECT TO RAMP GENERATOR LINE Q4, Q5, Q6, Q7, U15
U23-1 (EOS) IS ?
+ 4.9V
TROUBLE-SHOOT RAMP RESET CIRCUITS U6-8, 9, 10; U6-4, 5, 6; U14-12, 13
+ 0.1V
EOS OK
U16-7 (+ 4V REF) IS ?
≠ + 4V
TROUBLE-SHOOT + 4V REF U16-5, 6, 7
+ 4V
+ 4V REF OK
TROUBLE-SHOOT EOS CIRCUIT U23-1, 2, 3; Q9

Figure 6-7. Sweep Out Hung at 0 Vdc


NO SWEEP RAMP AT SWP OUT; SWP OUT HUNG AT ≈ +4 Vdc. SWEEP RAMP GENERATOR APPEARS TO BE IN "RAMP +4V" CONDITION
Q7-G (RAMP +4V) IS ?
THIS IS THE CORRECT +4V FALSE LEVEL
-7.7V
+3.6V
THIS IS THE "RAMP +4V TRUE LEVEL.
TROUBLE-SHOOT POSSIBLE LEAKY Q7
U28-1 (SET +4V) IS ?
+0.2V
+4.4V
"SET +4V" OK. NOW CHECK END OF SWEEP INPUT TO RAMP +4V CIRCUIT
SYSTEM HUNG IN SET STOP CYCLE GO TO SET STOP TROUBLE-SHOOTING (FIGURE 6-14)
U28-2 (EOS-IN) IS ?
+5V
EOS INPUT OK
IMPROPER EOS INPUT FOR CONT SWEEP MODE. TROUBLE-SHOOT U28-2 INPUT CIRCUITRY
TROUBLE-SHOOT RAMP +4V CIRCUIT U28-1, 2, 3; Q-1

NOTE: ALL VOLTAGE READINGS ARE APPROXIMATE. HOWEVER IF A CIRCUIT OUTPUT IS NOT NEAR EITHER VOLTAGE GIVEN, THEN THE PROBLEM IS IN THAT CIRCUIT.

Figure 6-8. No Sweep Ramp at SWP OUT


NO SWEEP RAMP AT SWP OUT; SWP OUT HUNG AT >4Vdc. SWEEP RAMP GENERATOR APPEARS TO HAVE RUN UP PAST THE NORMAL RESET LEVEL
U23-1 (EOS) IS ?
+4.9V
EOS BAD
+0.1V
EOS OK
U16-7 (+4V REF) IS ?
+4V REF OK
+4V
> +4V
Q6-B (RESET) IS ?
−0.6V
+0.7V
RAMP RESET OK
TROUBLE-SHOOT EOS CIRCUITS U23-1, 2, 3; Q9
+4V REF BAD. TROUBLE-SHOOT U16-5, 6, 7
RAMP RESET BAD. TROUBLE-SHOOT U6-8, 8 10; U6-4, 5, 6; U14-12, 13
TROUBLE-SHOOT Q5, Q6

NOTE: ALL VOLTAGE READINGS ARE APPROXIMATE. IF A CIRCUIT OUTPUT IS NOT NEAR EITHER VOLTAGE STATE GIVEN, THEN THE PROBLEM IS IN THAT CIRCUIT.

Figure 6-9. Sweep Ramp Hung at > +4V at SWP OUT

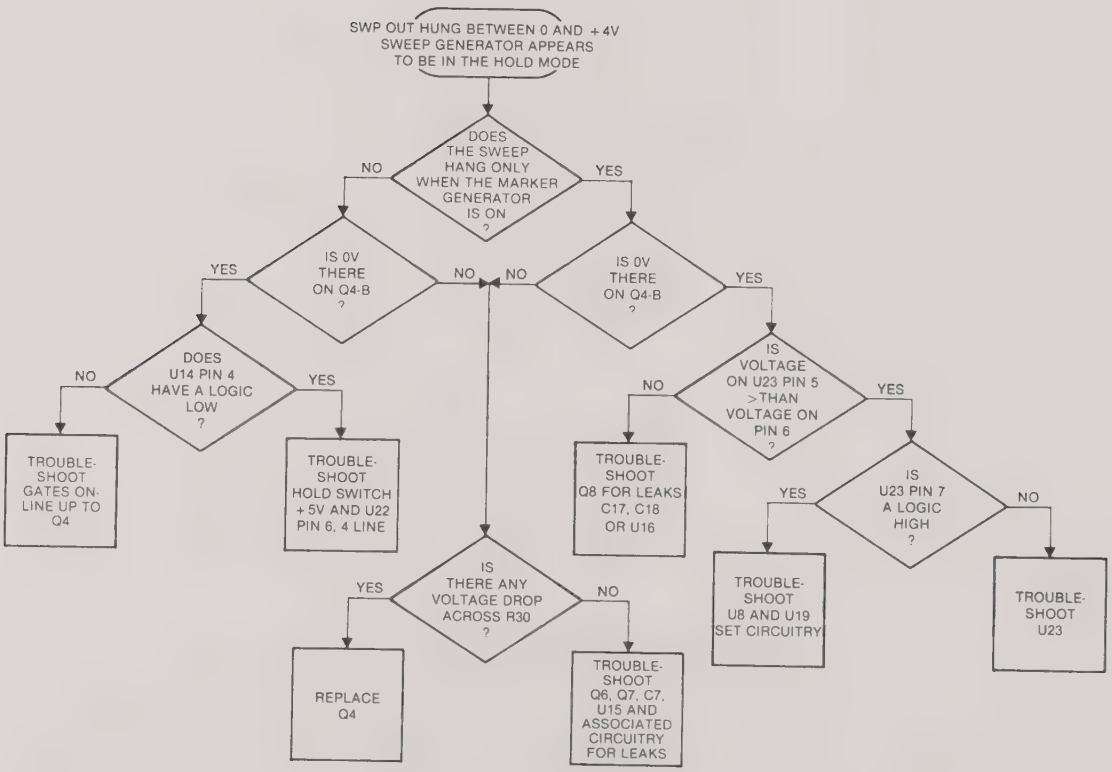
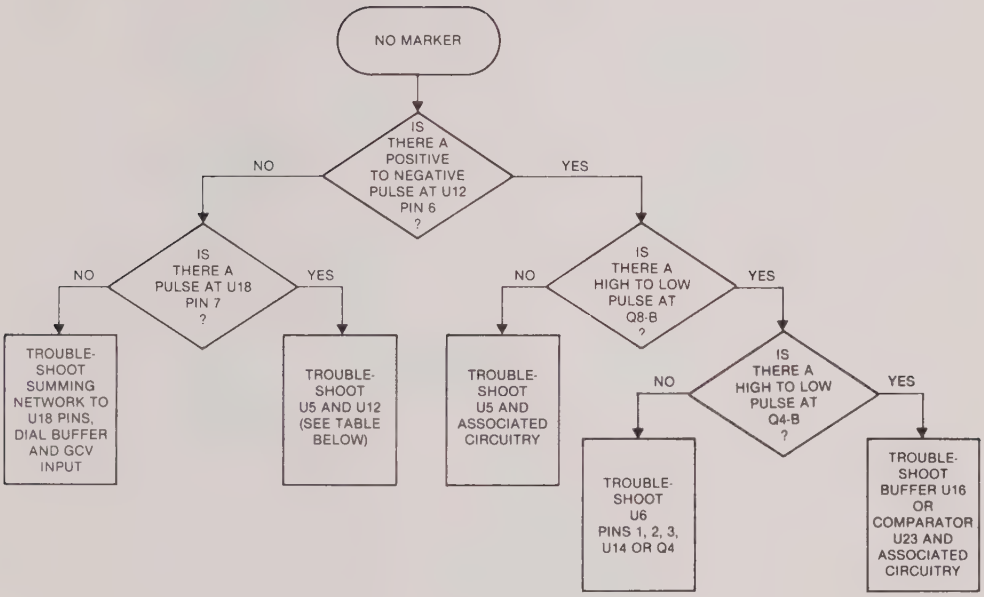


Figure 6-10. Sweep Out Voltage Hung Between 0 and +4V


NO MARKER
IS THERE A POSITIVE TO NEGATIVE PULSE AT U12 PIN 6 ?
NO
YES
IS THERE A PULSE AT U18 PIN 7 ?
NO
YES
TROUBLE-SHOOT SUMMING NETWORK TO U18 PINS, DIAL BUFFER AND GCV INPUT
TROUBLE-SHOOT U5 AND U12 (SEE TABLE BELOW)
IS THERE A HIGH TO LOW PULSE AT Q8-B ?
NO
YES
TROUBLE-SHOOT U5 AND ASSOCIATED CIRCUITRY
IS THERE A HIGH TO LOW PULSE AT Q4-B ?
NO
YES
TROUBLE-SHOOT U6 PINS 1, 2, 3, U14 OR Q4
TROUBLE-SHOOT BUFFER U16 OR COMPARATOR U23 AND ASSOCIATED CIRCUITRY

FOR FULL SWEEP OR SWEEP UP
U12 SHOULD MEASURE AS FOLLOWS:

PIN 13	LOW
PIN 3	LOW
PIN 9, 11	HIGH
PIN 10	SHOULD BE A PULSE
PIN 1, 2	LOW

FOR SWEEP DOWN
U12 SHOULD MEASURE

PIN 13	LOW
PIN 3, 5	HIGH
PIN 4	SHOULD BE A PULSE
PIN 11	LOW
PIN 1, 2	LOW

Figure 6-11. No Marker

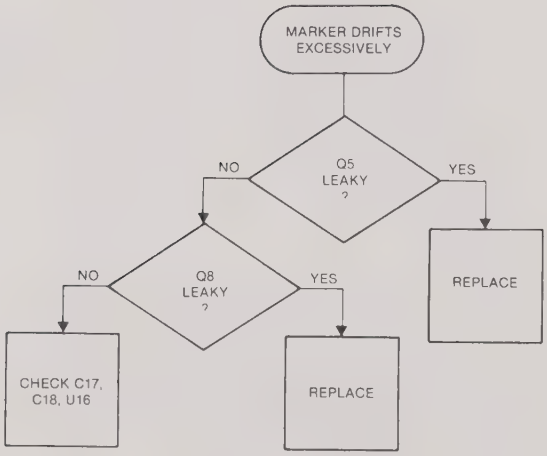
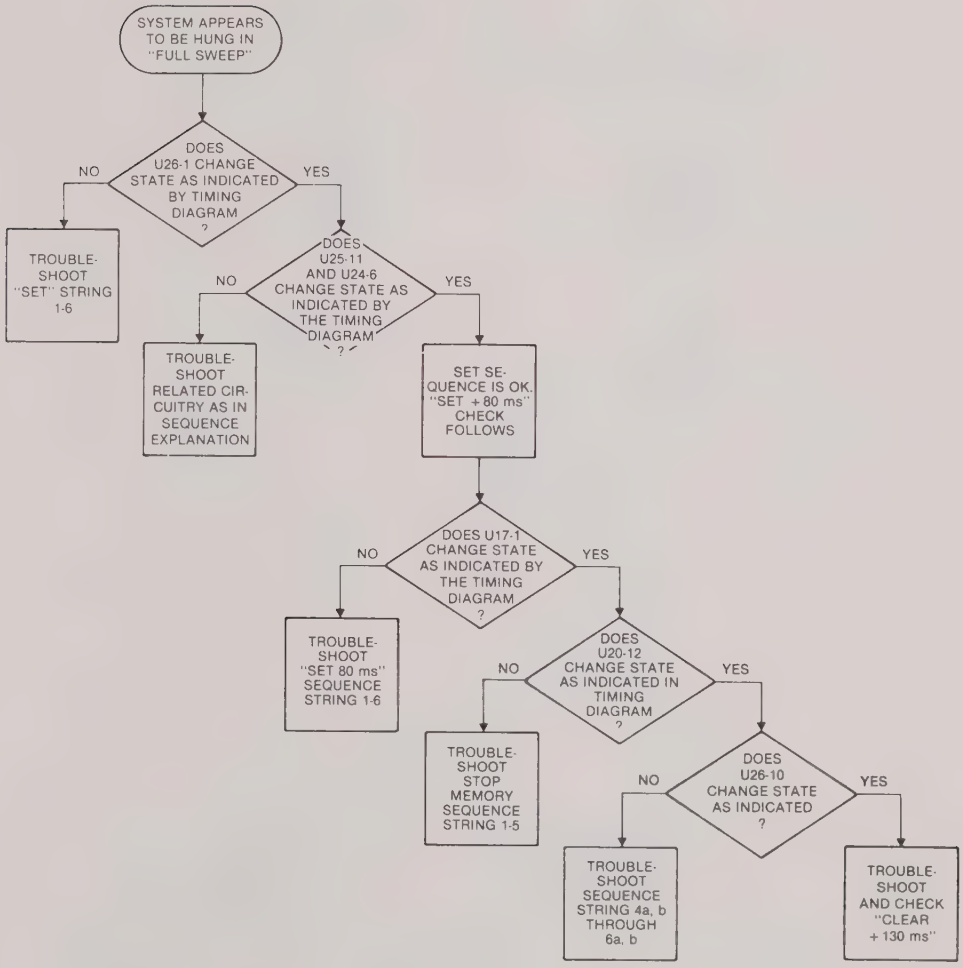
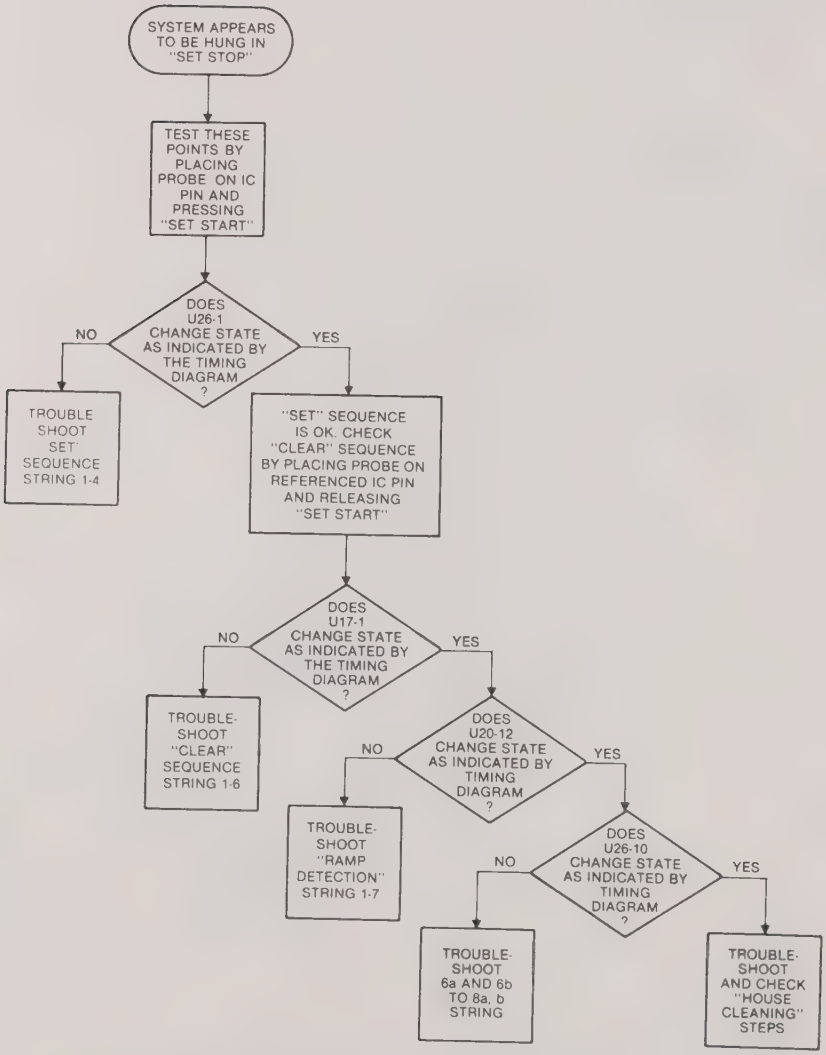


Figure 6-12. Marker Drifts Excessively


SYSTEM APPEARS TO BE HUNG IN "FULL SWEEP"
DOES U26-1 CHANGE STATE AS INDICATED BY TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "SET" STRING 1-6
DOES U25-11 AND U24-6 CHANGE STATE AS INDICATED BY THE TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT RELATED CIR-CUITRY AS IN SEQUENCE EXPLANATION
SET SE-QUENCE IS OK. "SET + 80 ms" CHECK FOLLOWS
DOES U17-1 CHANGE STATE AS INDICATED BY THE TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "SET 80 ms" SEQUENCE STRING 1-6
DOES U20-12 CHANGE STATE AS INDICATED IN TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT STOP MEMORY SEQUENCE STRING 1-5
DOES U26-10 CHANGE STATE AS INDICATED ?
NO
YES
TROUBLE-SHOOT SEQUENCE STRING 4a, b THROUGH 6a, b
TROUBLE-SHOOT AND CHECK "CLEAR + 130 ms"

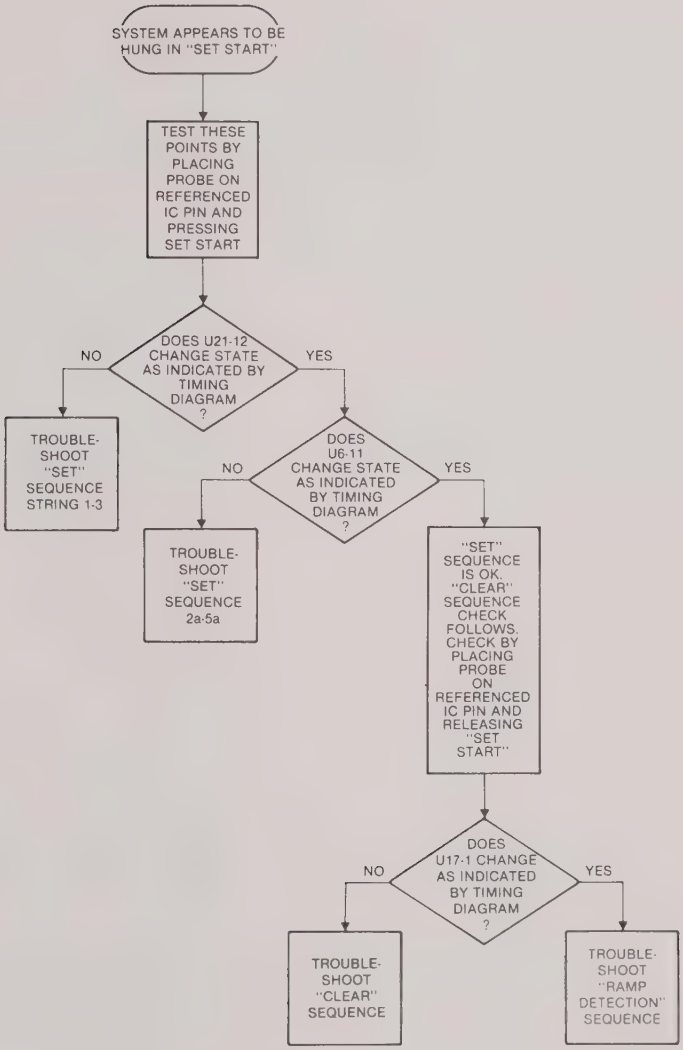
NOTES: 1. REFER TO APPENDIX A WHILE USING THIS TROUBLESHOOTING CHART.
2. TEST THESE POINTS BY PLACING PROBE ON REFERENCED IC PIN AND PRESSING FULL SWP.

Figure 6-13. System Hung Up In "Full Sweep"


SYSTEM APPEARS TO BE HUNG IN "SET STOP"
TEST THESE POINTS BY PLACING PROBE ON IC PIN AND PRESSING "SET START"
DOES U26-1 CHANGE STATE AS INDICATED BY THE TIMING DIAGRAM ?
NO
YES
TROUBLE SHOOT SET SEQUENCE STRING 1-4
"SET" SEQUENCE IS OK. CHECK "CLEAR" SEQUENCE BY PLACING PROBE ON REFERENCED IC PIN AND RELEASING "SET START"
DOES U17-1 CHANGE STATE AS INDICATED BY THE TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "CLEAR" SEQUENCE STRING 1-6
DOES U20-12 CHANGE STATE AS INDICATED BY TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "RAMP DETECTION" STRING 1-7
DOES U26-10 CHANGE STATE AS INDICATED BY TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT 6a AND 6b TO 8a, b STRING
TROUBLE-SHOOT AND CHECK "HOUSE CLEANING" STEPS

NOTE: REFER TO APPENDIX B WHILE USING THIS TROUBLESHOOTING CHART.

Figure 6-14. System Hung In Set Stop


SYSTEM APPEARS TO BE HUNG IN "SET START"
TEST THESE POINTS BY PLACING PROBE ON REFERENCED IC PIN AND PRESSING SET START
DOES U21-12 CHANGE STATE AS INDICATED BY TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "SET" SEQUENCE STRING 1-3
DOES U6-11 CHANGE STATE AS INDICATED BY TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "SET" SEQUENCE 2a-5a
"SET" SEQUENCE IS OK. "CLEAR" SEQUENCE CHECK FOLLOWS. CHECK BY PLACING PROBE ON REFERENCED IC PIN AND RELEASING "SET START"
DOES U17-1 CHANGE AS INDICATED BY TIMING DIAGRAM ?
NO
YES
TROUBLE-SHOOT "CLEAR" SEQUENCE
TROUBLE-SHOOT "RAMP DETECTION" SEQUENCE

NOTE: REFER TO APPENDIX C WHILE USING THIS TROUBLESHOOTING CHART.

Figure 6-15. System Appears To Be Hung In Set Start

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as develop ment and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to sumarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

Drawing	Drawing No.
Instrument Schematic	0004-00-0170
Generator Board Assembly	1100-00-0868
Generator Board Schematic	0103-00-0868
Generator Board Parts List	1100-00-0868
Sweep Baord Assembly	1100-00-0867
Sweep Board Schematic	0103-00-0867
Sweep Board Parts List	1100-00-0867
Chassis Assembly	0102-00-0869
Chassis Parts Lists	1101-00-0869

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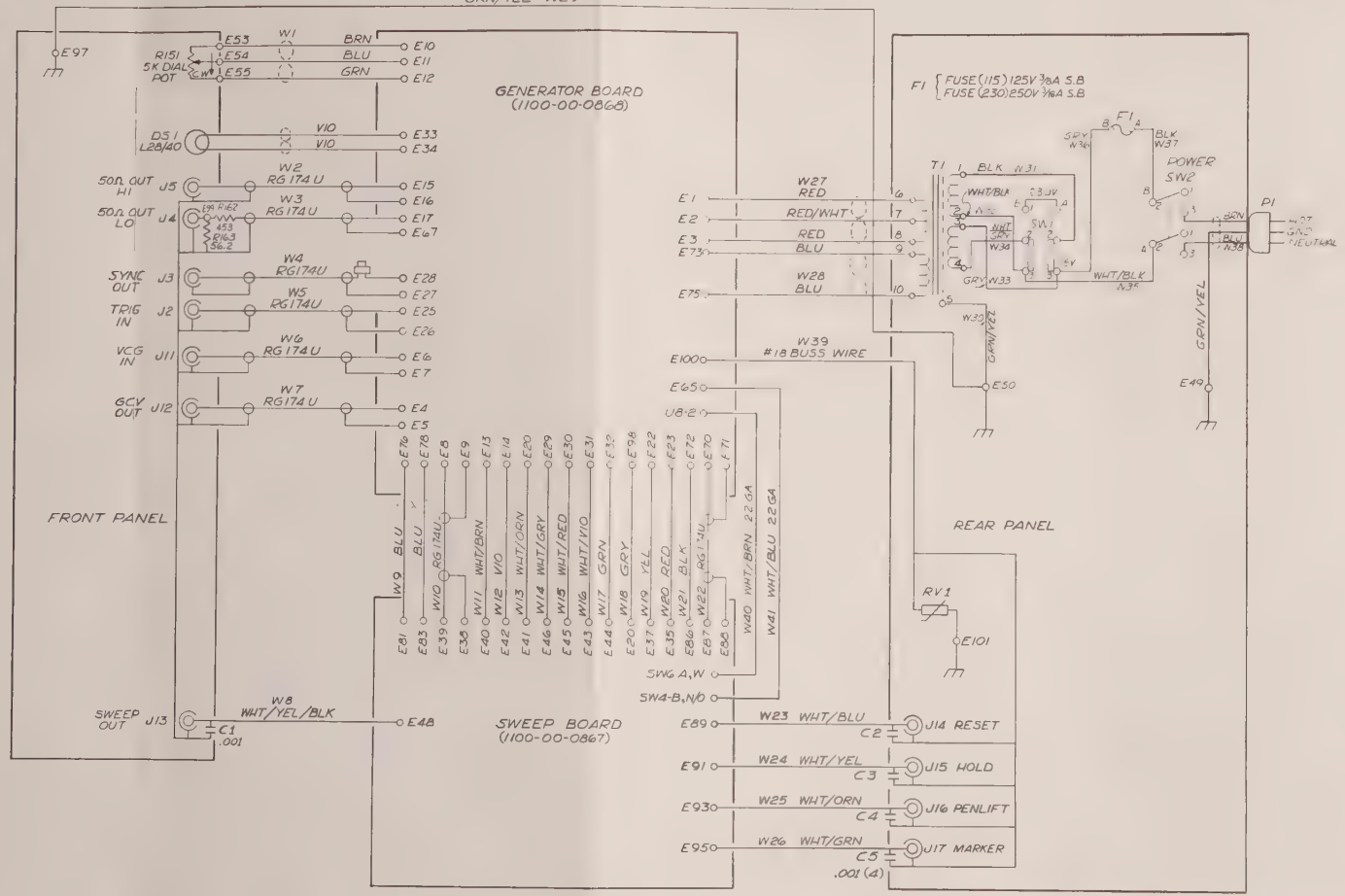
REV	ECN	BY	DATE	APP
B	2783	SC	7/2/81	



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 8/25/80	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	APPROVED	3-16-81	TITLE SCHEMATIC: INSTRUMENT
FINISH WAVETEK PROCESS	RELEASE APPROV.		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 189
	DO NOT SCALE DWG		DWG NO 0004-00-0170 REV B
	SCALE		CODE IDENT 23338 SHEET 1 OF 1

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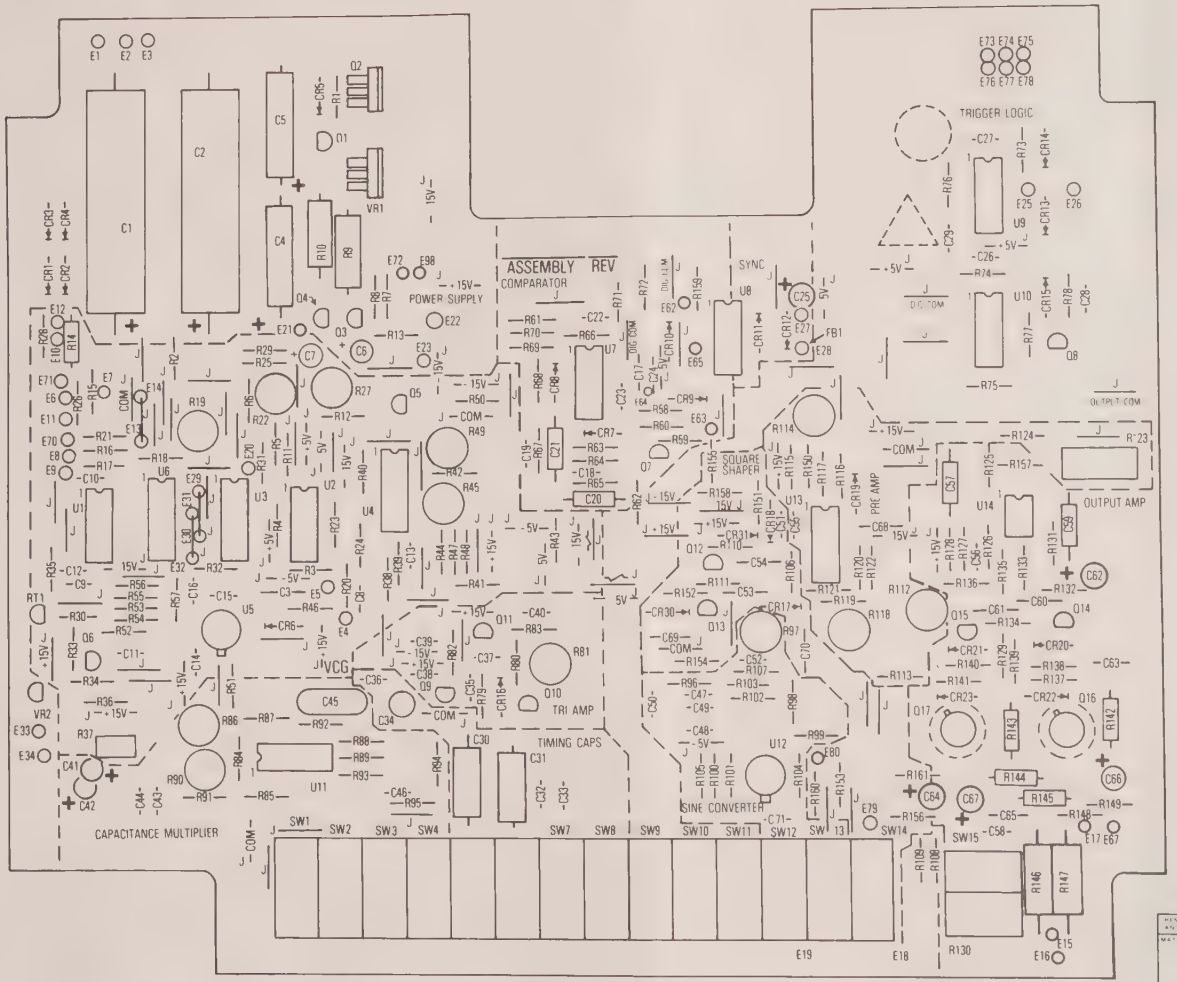
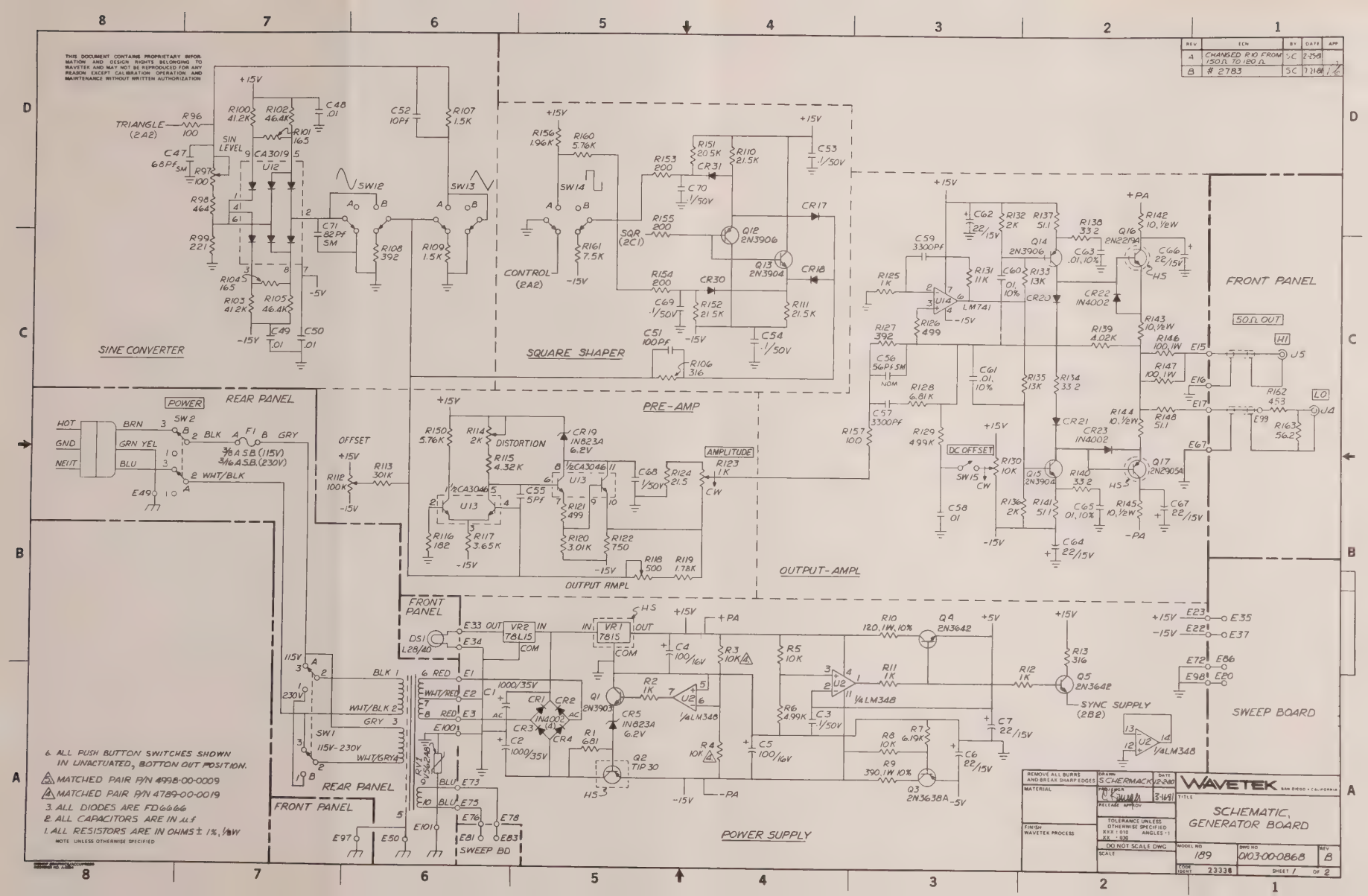


		WAVETEK	
		GENERATOR BOARD	
		MODEL NO. 189	DRG NO. 1100-00-0868
		COST CODE 23330	SHEET 1 OF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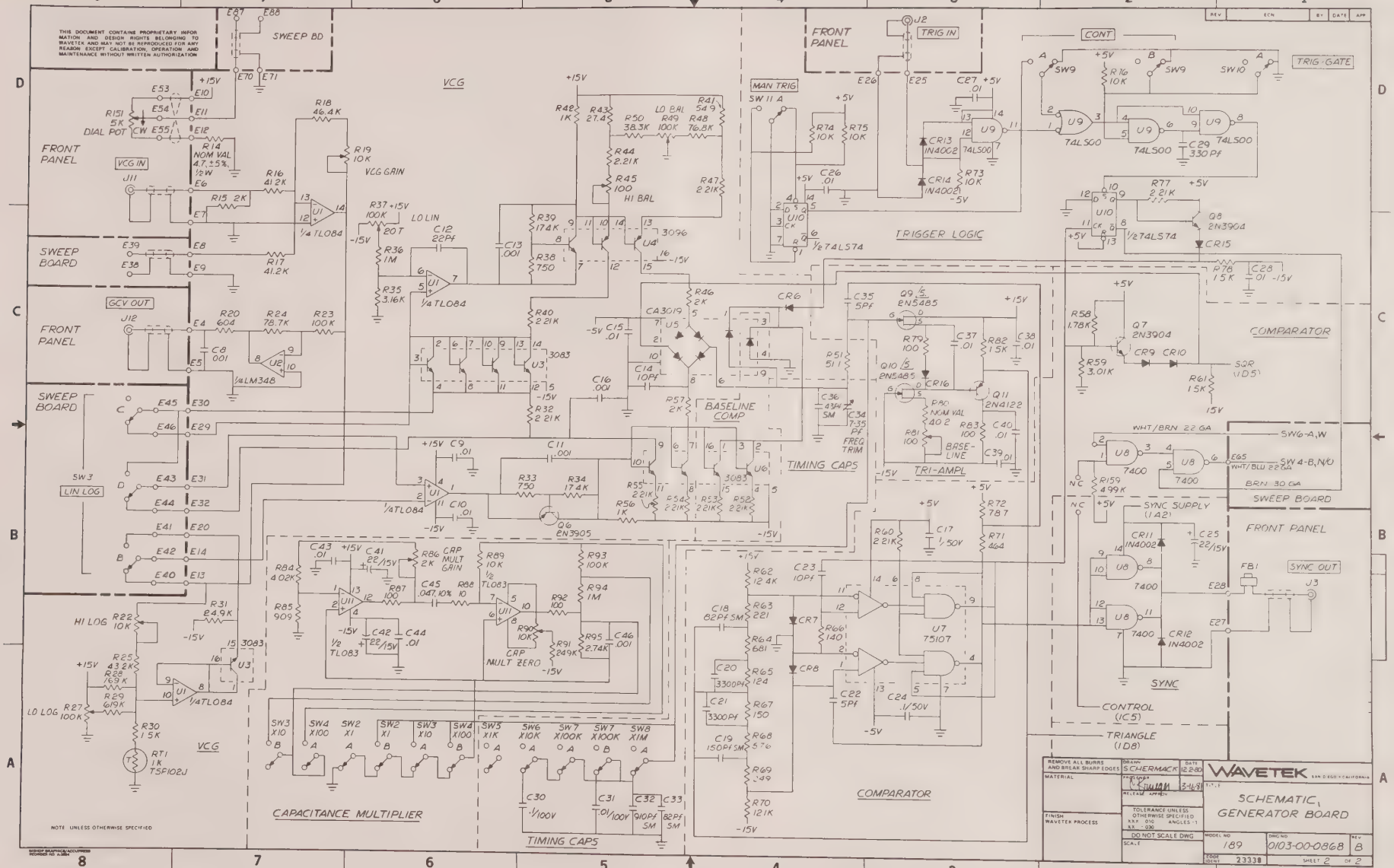
REV ECN BY DATE APP
A CHANGED R10 FROM 150Ω TO 180Ω SC 2-25-81
B # 2783 SC 7/28/81
SINE CONVERTER
SQUARE SHAPER
PRE-AMP
OUTPUT AMPL
OUTPUT-AMPL
POWER SUPPLY
REAR PANEL
FRONT PANEL
SWEEP BOARD
SYNC SUPPLY (2B2)
DC OFFSET
AMPLITUDE
OFFSET
TRIANGLE (2A2)
CONTROL (2A2)
SQR (2C1)
SIN LEVEL
50Ω OUT
HI
LO
6. ALL PUSH BUTTON SWITCHES SHOWN IN UNACTUATED, BOTTON OUT POSITION.
MATCHED PAIR P/N 4998-00-0009
MATCHED PAIR P/N 4789-00-0019
3. ALL DIODES ARE FD6666
2. ALL CAPACITORS ARE IN μf
1. ALL RESISTORS ARE IN OHMS ± 1%, ¼W
NOTE UNLESS OTHERWISE SPECIFIED
WAVETEK SAN DIEGO • CALIFORNIA
SCHEMATIC, GENERATOR BOARD
MODEL NO 189
DWG NO 0003-00-0868
REV B
SHEET 1 OF 2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SWEEP BD
VCG
FRONT PANEL
TRIG IN
CONT
TRIG GATE
MAN TRIG
TRIGGER LOGIC
VCG IN
VCG GAIN
LO LIN
HI BAL
LO BAL
DIAL POT
SWEEP BOARD
GCV OUT
BASELINE COMP
TIMING CAPS
TRI-AMPL
COMPARATOR
SYNC SUPPLY (1A2)
SYNC
SYNC OUT
CONTROL (1C5)
TRIANGLE (1D8)
LIN LOG
HI LOG
LO LOG
CAPACITANCE MULTIPLIER
CAP MULT GAIN
CAP MULT ZERO
NOTE UNLESS OTHERWISE SPECIFIED
SCHERMACK
WAVETEK
SCHEMATIC, GENERATOR BOARD
189
0103-00-0868
B
SHEET 2 OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG GENERATOR	0101-00-0868	WVTK	0101-00-0868	1
NONE	SCHEMATIC, GENERATOR	0103-00-0868	WVTK	0103-00-0868	1
C22 C35 C55	CAP.CER.5PF,1KV	DD-050	CRL	1500-00-5011	3
C14 C23 C52	CAP.CER.10PF,1KV	DD-100	CRL	1500-01-0011	3
C51	CAP.CER.100PF,1KV	DD-101	CRL	1500-01-0111	1
C11 C13 C16 C46 C8	CAP.CER., .001MF,1KV	DD-102	ARCO	1500-01-0211	5
C10 C15 C24 C27 C28 C37 C38 C29 C40 C43 C44 C48 C49 C50 C38 C9	CAP.CER., .01MF,50V	CK-103	CRL	1500-01-0310	16
C60 C61 C63 C65	CAP.CER.MN., .01MF,50V	1801X7R050A103K	VARDN	1500-01-0325	4
C17 C24 C3 C33 C54 C68 C69 C70	CAP.CER.MON., .1MF,50V	1802Z5U050A104Z	VARDN	1500-01-0405	8
C12	CAP.CER.22PF,1KV	DD-220	ARCO	1500-02-2011	1
C29	CAP.CER.330PF,1KV	DD-331	ARCO	1500-03-3111	1
C20 C21 C57 C59	CAP.C.MN.3300PF,50V	1801X7R050A332J	VRDYN	1500-03-3205	4
C19	CAP.MICA.150PF,500V	DM15-151J	ARCO	1500-11-5100	1
C36	CAP.MICA.43PF,500V	DM15-430J	ARCO	1500-14-3000	1
C56T	CAP.MICA.56PF,500V	DM15-560J	ARCO	1500-15-6000	1
C47	CAP.MICA.68PF,500V	DM15-680J	ARCO	1500-16-8000	1

WAVETEK PARTS LIST | TITLE PCA. GENERATOR | ASSEMBLY NO 1100-00-0868 | PAGE 1 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R112 R27 R49	POT. TRIM. 100K	91AR100K	BECK	4600-01-0402	3
R114 R86	POT. TRIM. 2K	91AR2K	BECK	4600-02-0201	2
R118	POT. TRIM. 500	91AR500	BECK	4600-05-0104	1
R130	POT. SWITCH 10K	GH-1879	CTS	4602-01-0300	1
R123	POT. CONT. 1K FROM 4600-01-0207	4609-71-0201	WVTK	4609-71-0201	1
R37	POT. TRIM. 20T. 100K	68WR100K	BECK	4609-90-0001	1
R142 R143 R144 R145	RES. C. 1/2W. 5%. 10	RC20GF-100	STKPL	4700-25-0100	4
R147	RES. C. 1/2W. 5%. 4.7	RC20GF-4R7	STKPL	4700-25-0479	1
R10	RES. C. 1W. 10%. 120	RC32F-121K	AB	4700-36-1200	1
R9	RES. C. 1W. 10%. 390	RC32GF391K	AB	4700-36-3900	1
R157 R79 R83 R87 R92 R96	RES. MF. 1/8W. 1%. 100	RN55D-1000F	TRW	4701-03-1000	6
R11 R12 R125 R2 R42 R56	RES. MF 1/8W. 1%. 1K	RN55D-1001F	TRW	4701-03-1001	6
R5 R73 R74 R75 R76 R8 R89	RES. MF. 1/8W. 1%. 10K	RN55D-1002F	TRW	4701-03-1002	7
R23 R93	RES. MF. 1/8W. 1%. 100K	RN55D-1003F	TRW	4701-03-1003	2
R36 R94	RES. MF 1/8W. 1%. 1M	RN55D-1004F	TRW	4701-03-1004	2

WAVETEK PARTS LIST | TITLE PCA. GENERATOR | ASSEMBLY NO 1100-00-0868 | PAGE 3 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R131	RES. MF. 1/8W. 1%. 20.5K	RN55D-2052F	TRW	4701-03-2052	1
R110 R111 R152	RES. MF. 1/8W. 1%. 21.5K	RN55D-2152F	TRW	4701-03-2152	3
R124T	RES. MF. 1/8W. 1%. 21.5	RN55D-21R5F	TRW	4701-03-2159	1
R83 R99	RES. MF. 1/8W. 1%. 221	RN55D-2210F	TRW	4701-03-2210	2
R34 R40 R44 R47 R52 R53 R54 R55 R60 R77	RES. MF. 1/8W. 1%. 2.21K	RN55D-2211F	TRW	4701-03-2211	10
R69	RES. MF. 1/8W. 1%. 249	RN55D-2490F	TRW	4701-03-2490	1
R31 R91	RES. MF. 1/8W. 1%. 24.9K	RN55D-2492F	TRW	4701-03-2492	2
R95	RES. MF. 1/8W. 1%. 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R43	RES. MF. 1/8W. 1%. 27.4	RN55D-27R4F	TRW	4701-03-2749	1
R120 R59	RES. MF. 1/8W. 1%. 3.01K	RN55D-3011F	TRW	4701-03-3011	2
R113	RES. MF. 1/8W. 1%. 301K	RN55D-3013F	TRW	4701-03-3013	1
R106 R13	RES. MF. 1/8W. 1%. 316	RN55D-3160F	TRW	4701-03-3160	2
R35	RES. MF. 1/8W. 1%. 3.16K	RN55D-3161F	TRW	4701-03-3161	1
R134 R138 R140	RES. MF. 1/8W. 1%. 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R117	RES. MF. 1/8W. 1%. 3.65K	RN55D-3651F	TRW	4701-03-3651	1
R30	RES. MF. 1/8W. 1%. 38.3K	RN55D-3832F	TRW	4701-03-3832	1
R108 R127	RES. MF. 1/8W. 1%. 392	RN55D-3920F	TRW	4701-03-3920	2

WAVETEK PARTS LIST | TITLE PCA GENERATOR | ASSEMBLY NO 1100-00-0868 | PAGE 5 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C18 C33T C71	CAP.MICA.82PF,500V	DM15-820J	ARCO	1500-18-2000	3
C32	CAP.910PF,100V.1%	DM15-911F	ARCO	1500-19-1101	1
C4 C5	CAP.ELECT.100MF,16V	500D107G016DC7	SPRAG	1500-31-0101	2
C1 C2	CAP ELECT. 1000MF,35V	39D108G035GL6	SPRAG	1500-31-0212	2
C31	CAP.POLYC.,.01MF,100V	PA2B103F	ELCUB	1500-41-0304	1
C30	CAP.POLYC.,.1MF,100V	PA2B104F	ELCUB	1500-41-0404	1
C45	CAP.MYLAR.,.047MF100V	225P47391WD3	SPRAG	1500-44-7314	1
C34	VARI.7-35PF,250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	1
C25 C41 C42 C6 C62 C64 C66 C67 C7	CAP.TANT 22MF,15V	196D226X9015MA1	SPRAG	1500-72-2601	9
NONE	GENERATOR BOARD	1700-00-0850	WVTK	1700-00-0850	1
DS1	LAMP	L28/40	NURA	2400-02-0017	1
NONE	SUPPORT TYRAP	RAMS-S3-M	PANDT	2800-00-0029	1
NONE	HEAT SINK	NF-207	WAKE	2800-11-0001	2
NONE	TRANSIPAD	10160	METRS	2800-11-0004	2
FB1	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	1
R45 R81 R97	POT. TRIM. 100	91AR100	BECK	4600-01-0103	3
R19 R22 R90	POT. TRIM. 10K	91AR10K	BECK	4600-01-0315	3

WAVETEK PARTS LIST | TITLE PCA. GENERATOR | ASSEMBLY NO 1100-00-0868 | PAGE 2 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R88	RES. MF. 1/8W. 1%. 10	RN55D-10R0F	TRW	4701-03-1009	1
R131	RES. MF. 1/8W. 1%. 11K	RN55D-1102F	TRW	4701-03-1102	1
R70	RES. MF. 1/8W. 1%. 12.1K	RN55D-1212F	TRW	4701-03-1212	1
R65	RES. MF. 1/8W. 1%. 124	RN55D-1240F	TRW	4701-03-1240	1
R62	RES. MF. 1/8W. 1%. 12.4K	RN55D-1242F	TRW	4701-03-1242	1
R133 R135	RES. MF. 1/8W. 1%. 13K	RN55D-1302F	TRW	4701-03-1302	2
R66	RES. MF 1/8W. 1%. 140	RN55D-1400F	TRW	4701-03-1400	1
R67	RES. MF. 1/8W. 1%. 150	RN55D-1500F	TRW	4701-03-1500	1
R107 R109 R30 R61 R78	RES. MF. 1/8W. 1%. 1.5K	RN55D-1501F	TRW	4701-03-1501	6
R101 R104	RES. MF. 1/8W. 1%. 165	RN55D-1650F	TRW	4701-03-1650	2
R28	RES. MF. 1/8W. 1%. 169K	RN55D-1693	TRW	4701-03-1693	1
R34 R39	RES. MF. 1/8W. 1%. 17.4K	RN55D-1742F	TRW	4701-03-1742	2
R119 R38	RES. MF. 1/8W. 1%. 1.78M	RN55D-1781F	TRW	4701-03-1781	2
R116	RES. MF. 1/8W. 1%. 182	RN55D-1820F	TRW	4701-03-1820	1
R136	RES. MF. 1/8W. 1%. 1.96M	RN55D-1961F	TRW	4701-03-1961	1
R153 R154 R155	RES. MF. 1/8W. 1%. 200	RN55D-2000F	TRW	4701-03-2000	3
R132 R136 R13 R46 R57	RES. MF. 1/8W. 1%. 2K	RN55D-2001F	TRW	4701-03-2001	5

WAVETEK PARTS LIST | TITLE PCA. GENERATOR | ASSEMBLY NO. 1100-00-0868 | PAGE 4 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R139 R84	RES MF. 1/8W. 1%. 4.02K	RN55D-4021F	TRW	4701-03-4021	2
R80T	RES. MF. 1/8W. 1%. 40.2	RN55D-40R2F	TRW	4701-03-4029	1
R100 R103 R16 R17	RES. MF. 1/8W. 1%. 41.2K	RN55D-4122F	TRW	4701-03-4122	4
R113	RES. MF. 1/8W. 1%. 4.32K	RN55D-4321F	TRW	4701-03-4321	1
R25	RES. MF. 1/8W. 1%. 43.2K	RN55D-4322F	TRW	4701-03-4322	1
R71 R98	RES. MF. 1/8W. 1% 464	RN55D-4640F	TRW	4701-03-4640	2
R102 R105 R18	RES. MF. 1/8W. 1%. 46.4K	RN55D-4642F	TRW	4701-03-4642	3
R121 R126	RES. MF. 1/8. 1%. 499	RN55D-4990F	TRW	4701-03-4990	2
R129 R139 R6	RES. MF. 1/8W. 1%. 4.99K	RN55D-4991F	TRW	4701-03-4991	3
R137 R141 R140 R51	RES. MF. 1/8W. 1%. 51.1	RN55D-51R1F	TRW	4701-03-5119	4
R41	RES. MF. 1/8W. 1%. 54.9	RN55D-54R9F	TRW	4701-03-5499	1
[illegible]	RES. MF. 1/8W. 1%. 576	RN55D-5760F	TRW	4701-03-5760	1
R150 R160	RES. MF. 1/8W. 1%. 5.76M	RN55D-5761F	TRW	4701-03-5761	2
R20	RES. MF. 1/8W. 1%. 604	RN55D-6040F	TRW	4701-03-6040	1
R7	RES. MF. 1/8W. 1%. 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R1 R64	RES. MF. 1/8W. 1%. 681	RN55D-6810F	TRW	4701-03-6810	2
R128	RES. MF. 1/8W. 1%. 6.81K	RN55D-6811F	TRW	4701-03-6811	1

WAVETEK PARTS LIST | TITLE PCA. GENERATOR | ASSEMBLY NO 1100-00-0868 | PAGE 6 | REV C

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE PARTS LIST PCA, GENERATOR BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 189 DWG NO 1100-00-0868 REV C
	DO NOT SCALE DWG		CODE IDENT 23338 SHEET 1 OF 2
	SCALE		

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R122 R33 R38	RES.MF 1/8W.1%.750	RN55D-7500F	TRW	4701-03-7500	3
R161	RES.MF.1/8W.1%.7.5K	RN55D-7501F	TRW	4701-03-7501	1
R48	RES.MF.1/8W.1%.76.8K	RN55D 7682F	TRW	4701-03-7682	1
R24	RES.MF.1/8W.1%.78.7K	RN55D-7872F	TRW	4701-03-7872	1
R72	RES.MF.1/8W.1%.78.7	RN55D 78R7F	TRW	4701-03-7879	1
R85	RES.MF.1/8W.1%.909	RN55D 9090F	TRW	4701-03-9090	1
R29	RES MF.1/4W.1%.6199	RN60D-6193F	TRW	4701-13-6193	1
R146 R147	RES.MF.1W.1%.100	RN70D-1000F	TRW	4701-33-1000	2
R3 R4	RES.SET.2-10K.1/8W QTY 2 4701-03-1002	142-501-64A	MVTH	4789-00-0019	1
CR19 CR5	DIODE.ZENER 6.2V	1N823A	NPC	4801-01-0823	2
CR1 CR11 CR12 CR13 CR14 CR2 CR22 CR23 CR3 CR4	DIODE	SCE-1	BEMT	4801-02-0001	10
CR10 CR15 CR16 CR17 CR18 CR20 CR21 CR30 CR31 CR6 CR7 CR8 CR9	DIODE	FD-6666	FAIR	4807-02-6666	13
Q16	TRANS	2N2219A	NSC	4901-02-2191	1
Q17	TRANS	2N2905A	NSC	4901-02-9051	1
Q3	TRANS	2N3638A	CARTR	4901-03-6381	1

WAVETEK PARTS LIST	TITLE PCA, GENERATOR	ASSEMBLY NO 1100-00-0868	REV C
		PAGE 7	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q4 Q5	TRANS	2N3642	FAIR	4901-03-6420	2
Q1	TRANS	2N3903	NSC	4901-03-9030	1
Q13 Q15 Q7 Q8	TRANS	2N3904	FAIR	4901-03-9040	4
Q6	TRANS	2N3905	FAIR	4901-03-9050	1
Q12 Q14	TRANS	2N3906	FAIR	4901-03-9060	2
Q11	TRANS	2N4122	NSC	4901-04-1220	1
Q10 Q9	TRANS.M/PR.2N5485 QTY 2 4901-05-4850	142-501-53	MVTH	4998-00-0009	1
NONE	SWITCH ASSY PB	5103-00-0039	MVTH	5103-00-0039	1
RT1	THERMISTER	TSP102J	TI	5300-00-0009	1
U11	IC	TL083CN	TI	7000-00-8300	1
U1	IC	TL084CN	TI	7000-00-8400	1
U2	IC	LM348N	NSC	7000-03-4800	1
U14	IC	MA-741	FAIR	7000-07-4100	1
U12 U5	IC	CA-3019	FAIR	7000-30-1900	2
U13	IC	CA-3046	RCA	7000-30-4600	1
U3 U6	IC	CA3080	FAIR	7000-30-8300	2
U4	IC	CA-3096AE	RCA	7000-30-9600	1

WAVETEK PARTS LIST	TITLE PCA, GENERATOR	ASSEMBLY NO 1100-00-0868	REV C
		PAGE 8	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
VR2	IC	78L15	TI	7000-78-1501	1
U7	IC	SN75107AN	TI	7007-51-0700	1
U8	IC	7400	TI	8000-74-0000	1
U9	IC	74L800	TI	8000-74-0010	1
U10	IC	74LS74	TI	8000-74-7410	1

WAVETEK PARTS LIST	TITLE PCA, GENERATOR	ASSEMBLY NO 1100-00-0868	REV C
		PAGE 9	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST PCA, GENERATOR BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 189 DWG NO 1100-00-0868 REV C
	DO NOT SCALE DWG		
	SCALE		FSCM IDENT 23338 SHEET 2 OF 2

BISHOP GRAPHICS/OCCUPRESS REORDER NO. 4-884

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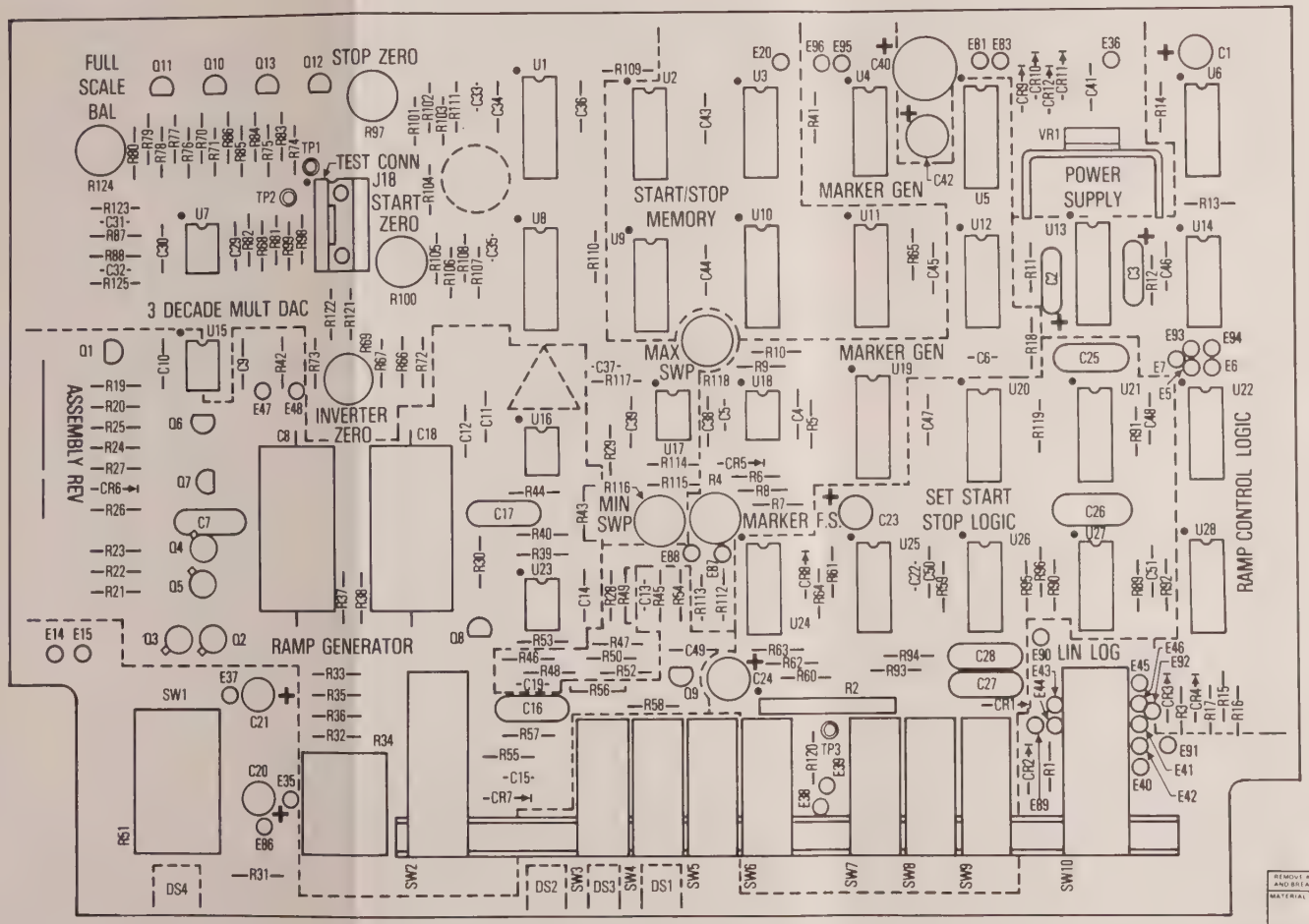
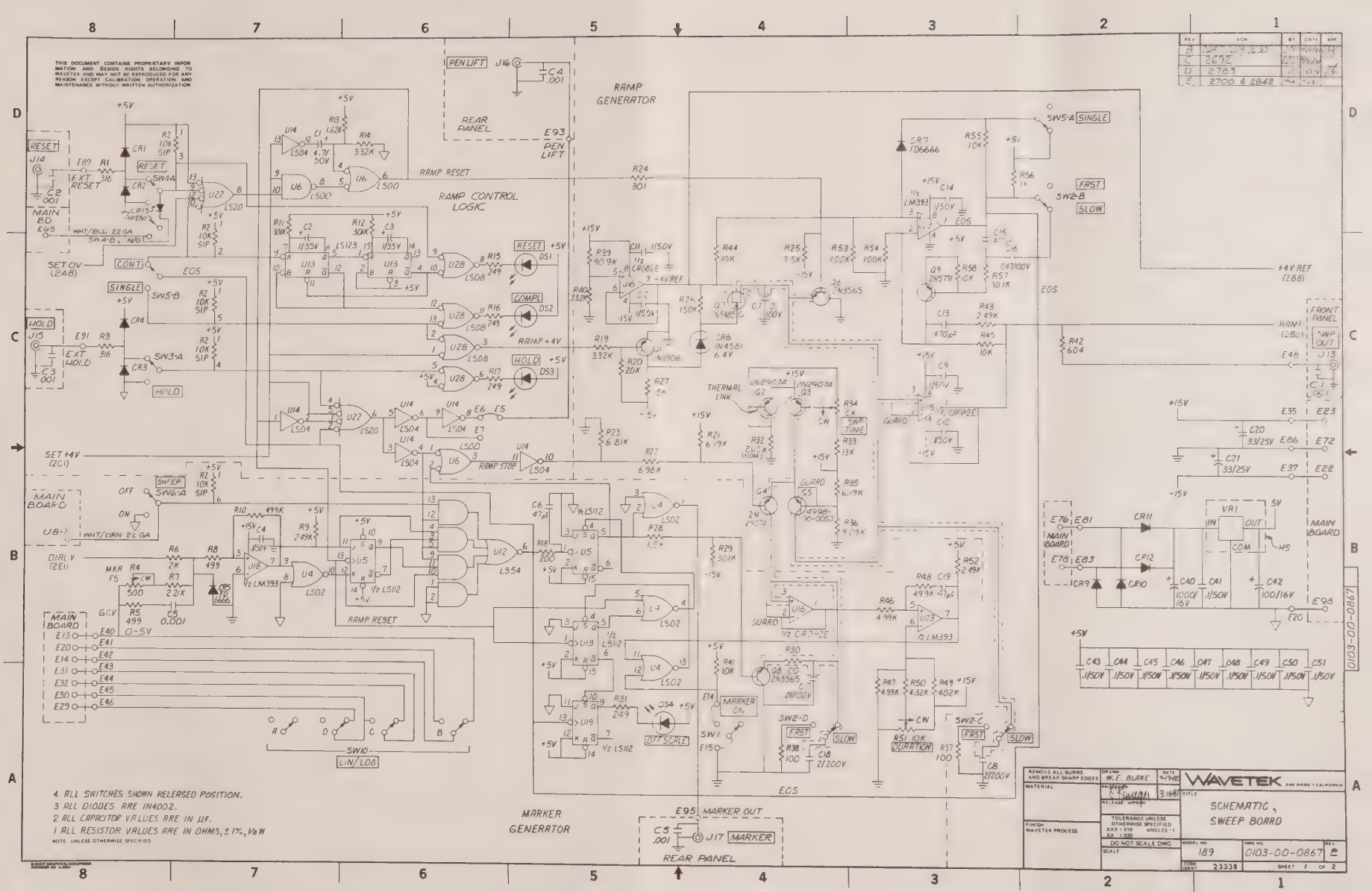


REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SWEEP BD
FINISH: WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010, XX ± .030, ANGLES ± 1		
	DO NOT SCALE DWG		MODEL NO: 189 — DWG NO: 1100-00-0867 — REV
	SCALE		CODE IDENT: 23338 — SHEET OF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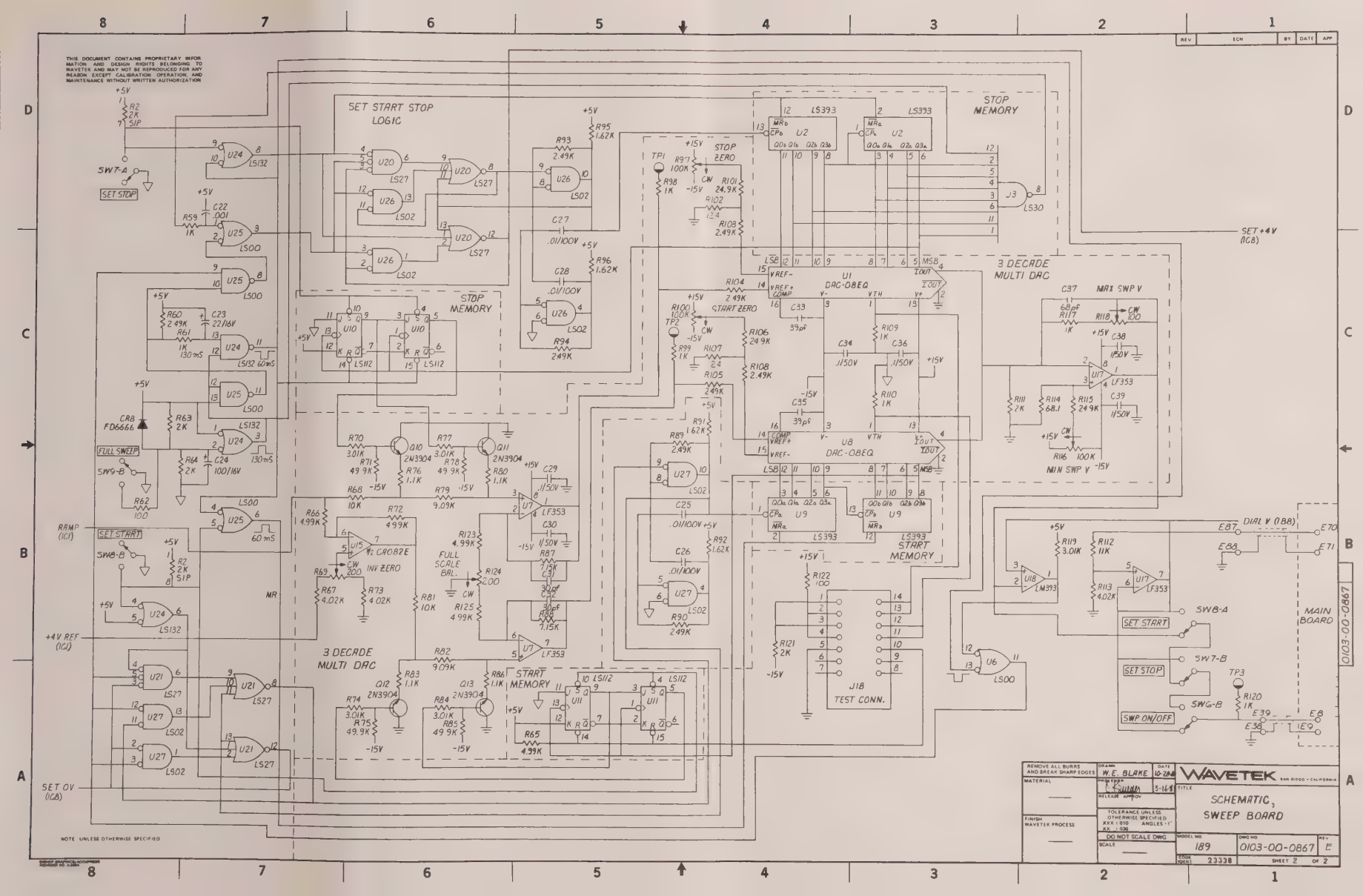
REV ECN BY DATE APP
B 2632
C 2632
D 2783
E 2700 & 2842
PEN LIFT J16
REAR PANEL
E93 PEN LIFT
RAMP GENERATOR
RAMP RESET
RAMP CONTROL LOGIC
RESET J14
HOLD J15
SET OV (2A8)
CONT
SINGLE
SET +4V (2C1)
SWEEP SW6-A
OFF
ON
MAIN BOARD U8-B
DIAL V (2E1)
MXR
GCV
MAIN BOARD
E13 E20 E14 E31 E32 E30 E29
E40 E41 E42 E43 E44 E45 E46
O-5V
SW10 LIN/LOG
RAMP STOP
RAMP +4V
SW5-A SINGLE
SW2-B FAST SLOW
+4V REF (2B8)
EOS
FRONT PANEL
MAIN BOARD
VR1
CR11 CR12 CR9 CR10
MARKER GENERATOR
E95 MARKER OUT
J17 MARKER
REAR PANEL
SW1
SW2-D
SW2-C
R51 10K DURATION
OFF SCALE
MARKER ON
4. ALL SWITCHES SHOWN RELEASED POSITION.
3 ALL DIODES ARE IN4002.
2 ALL CAPACITOR VALUES ARE IN µF.
1 ALL RESISTOR VALUES ARE IN OHMS, ± 1%, ⅛ W
NOTE UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN W.E. BLAKE 9-9-82
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1 XX ± 030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE SCHEMATIC, SWEEP BOARD
MODEL NO 189
DWG NO 0103-00-0867
REV E
CODE IDENT 23338
SHEET 1 OF 2
0103-00-0867


SET START STOP LOGIC
STOP MEMORY
START MEMORY
3 DECADE MULTI DAC
DAC-08EQ
TEST CONN.
J18
SET START
SET STOP
SWP ON/OFF
MAIN BOARD
SCHEMATIC, SWEEP BOARD
WAVETEK
0103-00-0867

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REV	E.N.	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, SWEEP BD	0101-00-0867	WVTK	0101-00-0867	1
NONE	SCHEMATIC, SWEEP BD	0103-00-0867	WVTK	0103-00-0867	1
C22 C5	CAP.CER., .001MF, 1KV	DD-102	ARCO	1500-01-0211	2
C10 C11 C12 C14 C29 C30 C34 C36 C38 C39 C4 C41 C43 C44 C45 C46 C47 C48 C49 C50 C51 C9	CAP,CER.MON., .1MF,50V	1B0225U050A104Z	VARDN	1500-01-0405	22
C31 C32	CAP CER 30PF,1KV	DD-300	CRL	1500-03-0091	2
C19 C6	CAP.CER 47PF,1KV	DD-470	ARCO	1500-04-7011	2
C13 C15	CAP,CER 470PF,1KV	DD-471	ARCO	1500-04-7111	2
C37	CAP,CER 68PF,1KV	DD-680	CRL	1500-06-8001	1
C33 J5	CAP MICA, 39PF,500V	DM15-390J	ARCO	1500-13-9000	2
C24 C44	CAP ELECT 100MF/16V RADIAL LEAD	CRE SERIES 100/16	CAPAR	1500-31-0111	2
C40	CAP ELECT,1000MF/16V RADIAL LEAD	CRE SERIES 1000/16	CAPAR	1500-31-0211	1
C20 C21	CAP ELECT 33MF 25V RADIAL LEAD	CLE SERIES 33/25	CAPAR	1500-33-3002	2
C1	CAP ELECT,4.7MF/50V RADIAL LEAD	CLE SERIES 4.7/50	CAPAR	1500-34-7903	1
C17 C25 C26 C27 C28	CAP,MYLAR, .01MF,100V	225P10391WD3	SPRAG	1500-41-0314	6

WAVETEK PARTS LIST — TITLE: PCA SWEEP BOARD — ASSEMBLY NO 1100-00-0867 — PAGE 1 — REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R109 R110 R117 R120 R56 R59 R61 R98 R99	RES.MF.1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	9
R41 R44 R45 R55 R58 R68 R81	RES.MF.1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	7
R53 R54	RES.MF.1/8W,1%,100K	RN55D-1003F	TRW	4701-03-1003	2
R76 R80 R83 R86	RES.MF.1/8W,1%,1.1K	RN55D-1101F	TRW	4701-03-1101	4
R112	RES.MF.1/8W,1%,11K	RN55D-1102F	TRW	4701-03-1102	1
R102 R107	RES.MF.1/8W,1%,124	RN55D-1240F	TRW	4701-03-1240	2
R33	RES.MF.1/8W,1%,13K	RN55D-1302F	TRW	4701-03-1302	1
R28	RES.MF.1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	1
R27	RES.MF.1/8W,1%,15K	RN55D-1502F	TRW	4701-03-1502	1
R26	RES.MF.1/8W,1%,150K	RN55D-1503F	TRW	4701-03-1503	1
R13 R91 R92 R95 R96	RES.MF.1/8W,1%,1.62K	RN55D-1621F	TRW	4701-03-1621	5
R18	RES.MF.1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	1
R111 R121 R6 R63 R64	RES.MF.1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	5
R20	RES.MF.1/8W,1%,20K	RN55D-2002F	TRW	4701-03-2002	1
R32T	RES.MF.1/8W,1%,21.5K	RN55D-2152F	TRW	4701-03-2152	1
R7	RES.MF.1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	1

WAVETEK PARTS LIST — TITLE: PCA SWEEP BOARD — ASSEMBLY NO 1100-00-0867 — PAGE 3 — REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R42	RES MF.1/8W,1%,604	RN55D-6040F	TRW	4701-03-6040	1
R21 R35	RES.MF.1/8W,1%,6.19K	RN55D-6191F	TRW	4701-03-6191	2
R23	RES.MF.1/8W,1%,6.81K	RN55D-6811F	TRW	4701-03-6811	1
R114	RES MF.1/8W,1%,68.1	RN55D-68R1F	TRW	4701-03-68R1	1
R24	RES.MF.1/8W,1%,6.98K	RN55D-6981F	TRW	4701-03-6981	1
R87 R90	RES.MF.1/8W,1%,7.15K	RN55D-7151F	TRW	4701-03-7151	2
R25	RES MF.1/8W,1%,7.5K	RN55D-7501F	TRW	4701-03-7501	1
R36 R79 R82	RES MF.1/8W,1%,9.09K	RN55D-9091F	TRW	4701-03-9091	3
R39	RES.MF.1/8W,1%,90.9K	RN55D-9092F	TRW	4701-03-9092	1
R49	RES MF.1/4W,1%,402K	RN60D 4023F	TRW	4701-13-4023	1
R2	RES MODULE	4310R-101-103	BOURN	4770-00-0008	1
CR6	DIODE	IN4581	MOT	4801-01-4581	1
CR1 CR10 CR11 CR12 CR2 CR3 CR4 CR9	DIODE	SCE 1	SEMT	4801-02-0001	8
CR5 CR7 CR8	DIODE	FD-6666	FAIR	4807-02-6666	3
CR13	DIODE	5082-2811	HP	4809-02-2811	1
DS1 DS2 DS3	LED GREEN	LD37-2	[illegible]	4899-00-0030	3
DS4	LED YELLOW	LD36-C	[illegible]	4899-00-0091	1

WAVETEK PARTS LIST — TITLE: PCA SWEEP BOARD — ASSEMBLY NO 1100-00-0867 — PAGE 5 — REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C7					
C18 C8	CAP.MYLR.2MF,200V	2MFW205K	AMRAD	1500-42 0504	2
C16	CAP.MYLAR..047MF100V	225P47391WD3	SPRAG	1500-44-7314	1
C2 C3	CAP.TANT.1MF.35V	150D105X9035A2	SPRAG	1500-71-0502	2
J23	CAP.TANT.22MF.15V	196D226X9015KA1	SPRAG	1500-72-2601	1
NONE	SWEEP BOARD	1700-00-0867	WVTK	1700-00-0867	1
J18	SKT.IC.14PIN	14-DIP	CINCH	2100-03-0011	1
NONE	TERM LOCK LUG	1414-4	SMITH	2100-04-0008	1
NONE	SOLDER LUG	1485-6	SMITH	2100-04-0023	1
TP1 TP2 TP3	BUSS BAR STANDOFF	2110-001	ARTUR	2100-05-0024	3
NONE	HEATSINK	371	AHAM	2800-11-0016	1
R118	POT.TRIM,100	91AR100	BECK	4600-01-0103	1
R34	POT.CONT.10K	72M1N0565103U	AB	4600-01-0322	1
R100 R116 R97	POT.TRIM.100K	91AR100K	BECK	4600-01-0402	3
R124 R69	POT.TRIM.200	91AR200	BECK	4600-02-0101	2
R4	POT.TRIM.500	91AR500	BECK	4600-05-0104	1
R31	POT SWITCH,10K	4602-01-0304	WVTK	4602-01-0304	1
R122 R30 R37 R38 R62	RES.MF 1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	5

WAVETEK PARTS LIST — TITLE: PCA SWEEP BOARD — ASSEMBLY NO 1100-00-0867 — PAGE 2 — REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R15 R16 R17 R31	RES.MF.1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	4
R103 R104 R105 R108 R43 R52 R60 R89 R9 R90 R93 R94	RES.MF.1/8W,1%,2.49K	RN55D-2491F	TRW	4701-03-2491	12
R101 R106 R115	RES.MF.1/8W,1%,24.9K	RN55D-2492F	TRW	4701-03-2492	3
R24	RES.MF.1/8W,1%,301	RN55D-3010F	TRW	4701-03-3010	1
R119 R70 R74 R77 R84	RES.MF.1/8W,1%,3.01K	RN55D-3011F	TRW	4701-03-3011	5
R29 R57	RES.MF.1/8W,1%,30.1K	RN55D-3012F	TRW	4701-03-3012	2
R11 R12	RES.MF.1/8W,1%,301K	RN55D-3013F	TRW	4701-03-3013	2
R1 R3	RES.MF.1/8W,1%,316	RN55D-3160F	TRW	4701-03-3160	2
R14 R19	RES.MF.1/8W,1%,3.32K	RN55D-3321F	TRW	4701-03-3321	2
R40	RES.MF.1/8W,1%,33.2K	RN55D-3322F	TRW	4701-03-3322	1
R113 R67 R73	RES.MF.1/8W,1%,4.02K	RN55D-4021F	TRW	4701-03-4021	3
R50	RES.MF.1/8W,1%,4.32K	RN55D-4321F	TRW	4701-03-4321	1
R5 R8	RES.MF.1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	2
R123 R125 R46 R47 R65 R66 R72	RES.MF.1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	7
R48 R71 R75 R78 R85	RES.MF.1/8W,1%,49.9K	RN55D-4992F	TRW	4701-03-4992	5
R10	RES.MF.1/8W,1%,499K	RN55D-4993F	TRW	4701-03-4993	1

WAVETEK PARTS LIST — TITLE: PCA, SWEEP BOARD — ASSEMBLY NO 1100-00-0867 — PAGE 4 — REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q2 Q3 Q4	TRANS,METAL CAN	2N2907A	NAT	4901-02-9071	3
Q6 Q8	TRANS	2N3563	FAIR	4901-03-5630	2
Q10 Q11 Q12 Q13	TRANS	2N3904	FAIR	4901-03-9040	4
Q1	TRANS	2N3906	FAIR	4901-03-9060	1
Q7	TRANS	2N5485	MOT	4901-03-4850	1
Q9	TRANS	2N5771	NSC	4901-05-7710	1
Q5	TRANS, SEL. 2N2907A QTY 1 4901-02-9071	4998-00-0050	WVTK	4998-00-0050	1
NONE	SWITCH ASSY PB	5103-00-0041	WVTK	5103-00-0041	1
NONE	THERMAL EQUALIZING LINK	259-18-25	WAKE	5300-00-0008	1
U1 U8	IC	DAC-08EQ	AML	7000-00-0800	2
U15 U16	IC	CA082E	RCA	7000-00-8200	2
U17 U7	IC	LF353N	NSC	7000-03-5300	2
U18 U23	IC	LM393N	NSC	7000-03-9300	2
U25 U6	IC	74LS00	TI	8000-74-0010	2
U26 U27 U4	IC	74LS02	TI	8000-74-0210	3
U24	IC	74LS04	TI	8000-74-0410	1

WAVETEK PARTS LIST — TITLE: PCA SWEEP BOARD — ASSEMBLY NO 1100-00-0867 — PAGE 6 — REV F

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, SWEEP BOARD
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 188 — DWG NO 1100-00-0867 — REV F
	DO NOT SCALE DWG		FSCM NO 23330 — SHEET 1 OF 2
	SCALE		

SIGNUP GRAPHICS/OCCUPIED SCHANGE NO. A-3884

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U28	IC	74LS08	TI	8000-74-0810	1
U22	IC	74LS20	TI	8000-74-2010	1
U20 U21	IC	74LS27	TI	8000-74-2710	2
U3	IC	74LS30	BIG	8000-74-3010	1
U12	IC	74LS54	TI	8000-74-5410	1
VR1	VOLTAGE REGULATOR	7805393	FAIR	8000-78-0500	1
U10 U11 U19 U5	IC	74LS112	TI	8007-41-1210	4
U13	IC	74LS123B	BIG	8007-41-2310	1
U24	IC	74LS132	TI	8007-41-3210	1
U2 U9	IC	74LS393	TI	8007-43-9310	2

WAVETEK PARTS LIST	TITLE PCA, SWEEP BOARD	ASSEMBLY NO 1100-00-0867 PAGE 7	REV F

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST PCA, SWEEP BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 189 DWG NO 1100-00-0867 REV F
	DO NOT SCALE DWG		CODE IDENT 23338 SHEET 2 OF 2
	SCALE		

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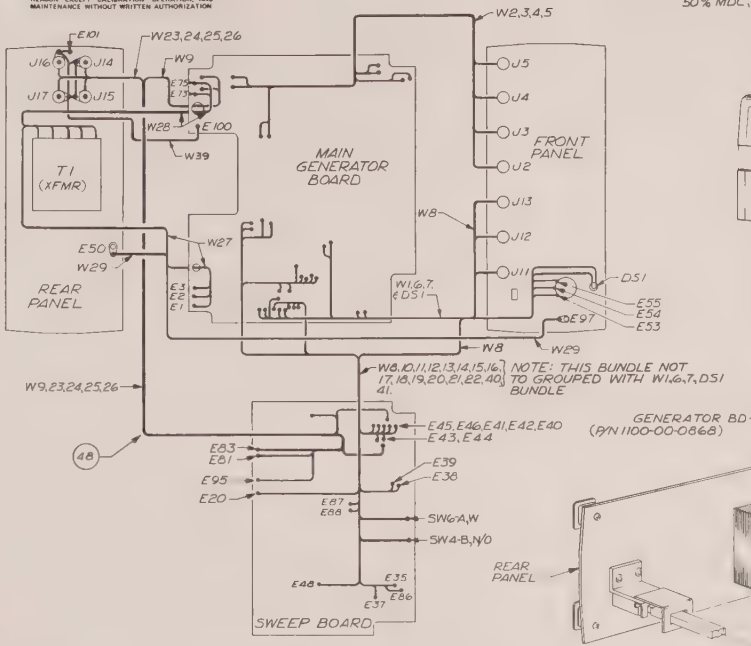
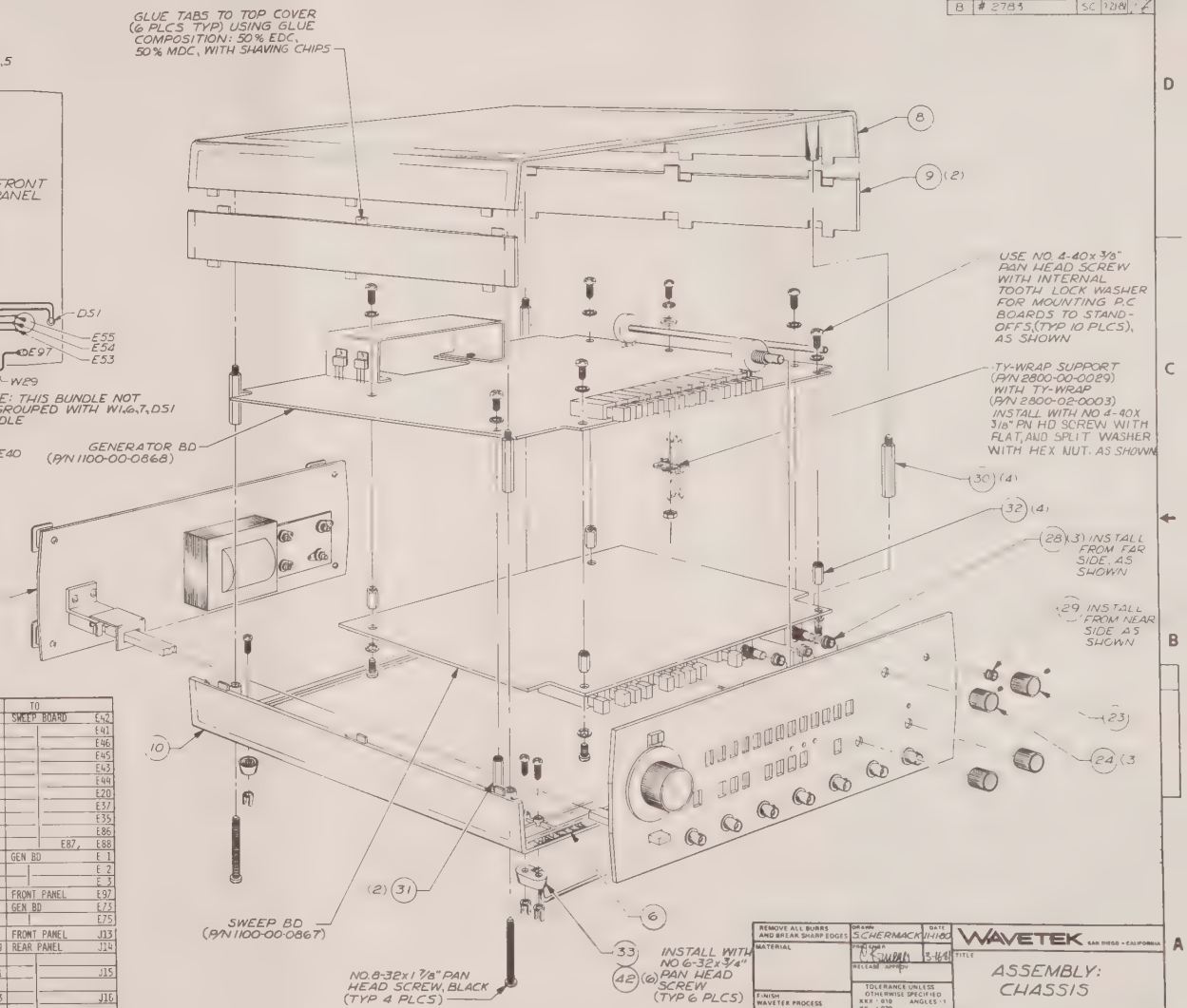
REV	ECN	BY	DATE	APP
B	# 2783	SC	7/84	




GLUE TABS TO TOP COVER (6 PLCS TYP) USING GLUE COMPOSITION: 50% EDC, 50% MDC, WITH SHAVING CHIPS
USE NO. 4-40 x 3/8" PAN HEAD SCREW WITH INTERNAL TOOTH LOCK WASHER FOR MOUNTING P.C BOARDS TO STAND-OFFS, (TYP 10 PLCS), AS SHOWN
TY-WRAP SUPPORT (P/N 2800-00-0029) WITH TY-WRAP (P/N 2800-02-0003) INSTALL WITH NO 4-40 X 3/8" PN HD SCREW WITH FLAT, AND SPLIT WASHER WITH HEX NUT. AS SHOWN
GENERATOR BD (P/N 1100-00-0868)
REAR PANEL
8
9 (2)
30 (4)
32 (4)
28 (3) INSTALL FROM FAR SIDE AS SHOWN
29 INSTALL FROM NEAR SIDE AS SHOWN
23
24 (3)
10
(2) 31
6
33
42 (6)
SWEEP BD (P/N 1100-00-0867)
NO.8-32 x 1 7/8" PAN HEAD SCREW, BLACK (TYP 4 PLCS)
INSTALL WITH NO 6-32 x 3/4" PAN HEAD SCREW (TYP 6 PLCS)

CHASSIS WIRING LIST

REF DES.	COLOR	FROM		TO	
W1	BRN	GEN BD	E10	FRONT PANEL	E53
	BLU		E11		E54
	GRN		E12		E55
W2	COAX		E15, E16		J 5
W3			E17, E67		J 4
W4			E28, E27		J 3
W5			E25, E26		J 2
W6			E 6, E 7		J11
W7			E 4, E 5		J12
W9	BLU		E76	SWEEP BOARD	E81
	BLU		E78		E85
W10	COAX		E 8, E 9		E39, E38
W11	W/BRN		E13		E40
W41	W/GRN		E36		SW6-A,W
W41	W/BLU		E35		SW4-B,N O

REF DES.	CO.OR	FROM		TO	
W12	V10	GEN BD	E14	SWEEP BOARD	E42
W13	W/ORN		E20		E41
W14	W/GRY		E29		E46
W15	W/RED		E30		E45
W16	W/V10		E31		E43
W17	GRN		E32		E44
W18	GRY		E98		E20
W19	YEL		E22		E37
W20	RED		E23		E35
W21	BLK		E72		E86
W22	COAX		E70, E71	E87,	E88
W27	RED	REAR PANEL	T1-6	GEN BD	E 1
	W/RED		T1-7		E 2
	RED		T1-8		E 3
W29	GRN/YEL	REAR PANEL	E50	FRONT PANEL	E97
W28	BLU	REAR PANEL	T1-9	GEN BD	E73
	BLU		T1-10		E75
W8	WHT/YEL/BLK		E48,	FRONT PANEL	J13
W23	W/BLU		E89	REAR PANEL	J14
W24	W/YEL		E91		J15
W25	W/ORN		E93		J16
	W/GRN		E95		J17
W39		REAR PANEL	J17	GEN BD	E100

⚠ NO. 6-32x2" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER, HEX NUT, CABLE CLAMP (ITEM NO. 27), FLAT WASHER, SPLIT LOCK WASHER, AND HEX NUT, AS SHOWN.
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN SCHERMACK 11-14-02
CHECKED 3-14-84
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO - CALIFORNIA

TITLE
ASSEMBLY: CHASSIS

MODEL NO	DWG NO	REV
189	0102-00-0869	B
DRAWING 23338	SHEET 1 OF 2	

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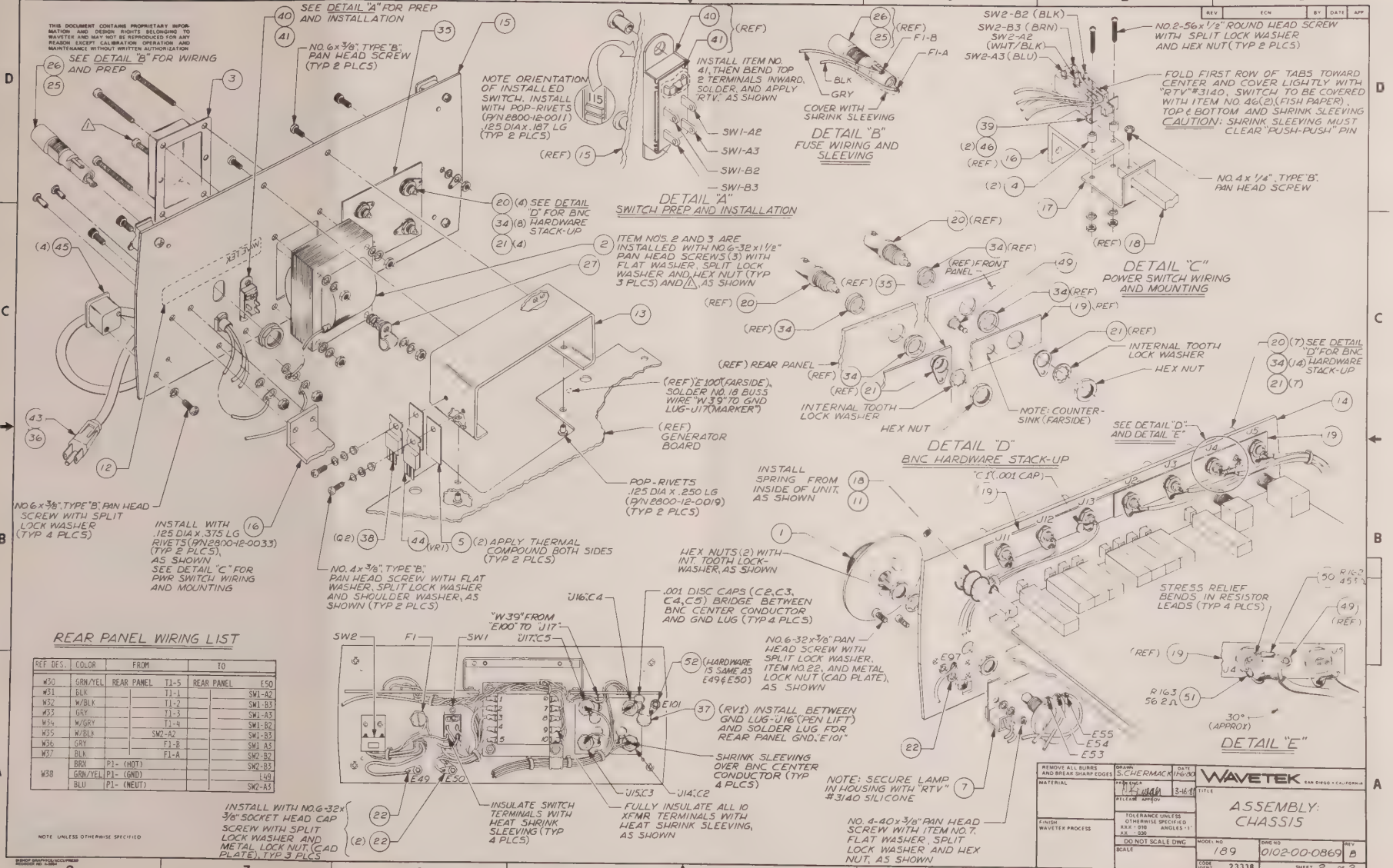

SEE DETAIL "A" FOR PREP AND INSTALLATION
SEE DETAIL "B" FOR WIRING AND PREP
NO. 6 x 3/8", TYPE "B", PAN HEAD SCREW (TYP 2 PLCS)
NOTE ORIENTATION OF INSTALLED SWITCH. INSTALL WITH POP-RIVETS (P/N 8800-12-0011) .125 DIA x .187 LG (TYP 2 PLCS)
INSTALL ITEM NO. 41, THEN BEND TOP 2 TERMINALS INWARD, SOLDER, AND APPLY "RTV" AS SHOWN
SW1-A2
SW1-A3
SW1-B2
SW1-B3
DETAIL "A" SWITCH PREP AND INSTALLATION
SW2-B2 (BLK)
SW2-B3 (BRN)
SW2-A2 (WHT/BLK)
SW2-A3 (BLU)
F1-B
F1-A
BLK
GRY
COVER WITH SHRINK SLEEVING
DETAIL "B" FUSE WIRING AND SLEEVING
NO. 2-56 x 1/2" ROUND HEAD SCREW WITH SPLIT LOCK WASHER AND HEX NUT (TYP 2 PLCS)
FOLD FIRST ROW OF TABS TOWARD CENTER AND COVER LIGHTLY WITH "RTV" #3140, SWITCH TO BE COVERED WITH ITEM NO. 46 (2), (FISH PAPER), TOP & BOTTOM AND SHRINK SLEEVING
CAUTION: SHRINK SLEEVING MUST CLEAR "PUSH-PUSH" PIN
NO. 4 x 1/4", TYPE "B", PAN HEAD SCREW
(4) SEE DETAIL "D" FOR BNC HARDWARE STACK-UP
(8) HARDWARE STACK-UP
ITEM NOS. 2 AND 3 ARE INSTALLED WITH NO. 6-32 x 1 1/2" PAN HEAD SCREWS (3) WITH FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT (TYP 3 PLCS) AND ⚠, AS SHOWN
(REF) FRONT PANEL
DETAIL "C" POWER SWITCH WIRING AND MOUNTING
(REF) REAR PANEL
INTERNAL TOOTH LOCK WASHER
HEX NUT
NOTE: COUNTER-SINK (FARSIDE)
(REF) E100 (FARSIDE), SOLDER NO. 18 BUSS WIRE "W39" TO GND LUG-J17 (MARKER)
(REF) GENERATOR BOARD
POP-RIVETS .125 DIA x .250 LG (P/N 8800-12-0019) (TYP 2 PLCS)
(2) APPLY THERMAL COMPOUND BOTH SIDES (TYP 2 PLCS)
NO. 6 x 3/8", TYPE "B", PAN HEAD SCREW WITH SPLIT LOCK WASHER (TYP 4 PLCS)
INSTALL WITH .125 DIA x .375 LG RIVETS (P/N 2800-12-0033) (TYP 2 PLCS), AS SHOWN
SEE DETAIL "C" FOR PWR SWITCH WIRING AND MOUNTING
NO. 4 x 3/8", TYPE "B", PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER AND SHOULDER WASHER, AS SHOWN (TYP 2 PLCS)
INSTALL SPRING FROM INSIDE OF UNIT, AS SHOWN
DETAIL "D" BNC HARDWARE STACK-UP
C1 (.001 CAP)
SEE DETAIL "D" AND DETAIL "E"
HEX NUTS (2) WITH INT. TOOTH LOCK-WASHER, AS SHOWN
.001 DISC CAPS (C2, C3, C4, C5) BRIDGE BETWEEN BNC CENTER CONDUCTOR AND GND LUG (TYP 4 PLCS)
"W39" FROM "E100" TO "J17"
NO. 6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER, ITEM NO. 22, AND METAL LOCK NUT (CAD PLATE), AS SHOWN
STRESS RELIEF BENDS IN RESISTOR LEADS (TYP 4 PLCS)
R163 56.2Ω
R160 45.3Ω
30° (APPROX)
DETAIL "E"
(HARDWARE IS SAME AS E49 & E50)
(RV1) INSTALL BETWEEN GND LUG-J16 (PEN LIFT) AND SOLDER LUG FOR REAR PANEL GND. "E101"
SHRINK SLEEVING OVER BNC CENTER CONDUCTOR (TYP 4 PLCS)
NOTE: SECURE LAMP IN HOUSING WITH "RTV" #3140 SILICONE
NO. 4-40 x 3/8" PAN HEAD SCREW WITH ITEM NO. 7, FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT, AS SHOWN
INSTALL WITH NO. 6-32 x 3/8" SOCKET HEAD CAP SCREW WITH SPLIT LOCK WASHER AND METAL LOCK NUT (CAD PLATE), TYP 3 PLCS
INSULATE SWITCH TERMINALS WITH HEAT SHRINK SLEEVING (TYP 4 PLCS)
FULLY INSULATE ALL 10 XFMR TERMINALS WITH HEAT SHRINK SLEEVING, AS SHOWN
SW2
F1
SW1
J17:C5
J16:C4
J15:C3
J14:C2
E49
E50
E101
E97
E98
E99
E55
E54
E53

REAR PANEL WIRING LIST

REF DES.	COLOR	FROM		TO	
		REAR PANEL	T1-5	REAR PANEL	E50
W30	GRN/YEL		T1-1		SW1-A2
W31	BLK		T1-2		SW1-B3
W32	W/BLK		T1-3		SW1-A3
W33	GRY		T1-4		SW1-B2
W34	W/GRY		SW2-A2		SW1-B3
W35	W/BLK		F1-B		SW1 A3
W36	GRY		F1-A		SW2-B2
W37	BLK				SW2-B3
W38	BRN	P1- (HOT)			L49
	GRN/YEL	P1- (GND)			SW2-A3
	BLU	P1- (NEUT)			

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. CHERMACK 11-6-80
APPROVED 3-16-81
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: ASSEMBLY: CHASSIS

MODEL NO. 189
DWG NO. 0102-00-0869
REV B
CODE IDENT NO. 23338
SHEET 2 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. CHASSIS	0102-00-0869	WVTK	0102-00-0869	1
1	DIAL ASSY	188-0029	WVTK	1201-00-0029	1
2	TRANSFORMER	5600-00-0025	WVTK	1204-00-0046	1
48	CHASSIS CABLE KIT	189-0878	WVTK	1207-00-0878	1
3	END BELL	110-333	WVTK	1400-00-0174	1
4	SPACER	8480	WVTK	1400-00-0653	2
5	INSULATOR. MICA	142-311	WVTK	1400-00-2080	2
6	PLATE. NAME	139-305	WVTK	1400-00-2180	1
7	INDICATOR. DIAL	180-303	WVTK	1400-00-4970	1
8	COVER. TOP	180-300-1	WVTK	1400-00-5000	1
9	EXPANDER	180-301	WVTK	1400-00-5010	2
45	POST	180-302	WVTK	1400-00-5020	4
10	COVER. BOTTOM	180-300-2	WVTK	1400-00-5030	1
11	SPRING. POWER ROD REF 3200-01-0001	1400-00-8280	WVTK	1400-00-8280	1
46	INSULATOR. PWR SWITCH REF 1600-99-0001	1400-00-8370	WVTK	1400-00-8370	2
13	BRACKET. AC SHIELD	1400-00-9473	WVTK	1400-00-9473	1
14	PANEL. FRONT	1400-01-3200	WVTK	1400-01-3200	1

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO 1101-00-0869 PAGE 1 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
15	PANEL. REAR	1400-01-3210	WVTK	1400-01-3210	1
16	BRACKET. SWITCH MNTG	1400-01-3263	WVTK	1400-01-3263	1
17	BRACKET. POWER ROD	1400-01-3273	WVTK	1400-01-3273	1
18	POWER ROD	1400-01-3280	WVTK	1400-01-3280	1
19	GROUNDING. PLATE	1400-01-3313	WVTK	1400-01-3313	2
35	PLATE. BNC GROUNDING	1400-01-3953	WVTK	1400-01-3953	1
12	LABEL. RATING	1400-01-4610	WVTK	1400-01-4610	1
C1 C2 C3 C4 C5	CAP. CER. .001MF. 1KV	DD-102	ARCO	1500-01-0211	5
20	BNC CONN	KC-7946	KING	2100-01-0002	11
52	TERM. LOCK LUG	1414-6	SMITH	2100-04-0009	1
21	SOLDER LUG	1497	SMITH	2100-04-0012	11
22	SOLDER LUG	1485-6	SMITH	2100-04-0025	4
49	TERMINAL. INSULATED	014-2001-00-0-479	SLTRO	2100-05-0054	1
23	KNOB. SMALL	0-M-9	ROGAN	2400-01-0010	1
24	KNOB. 1/4IN BUSHING	RB-67-0-M-9	ROGAN	2400-01-0017	3
25	FUSE. 3/8A. 250V. 6-8	MDL 3/8	BUSMN	2400-05-0004	1
26	FUSE HOLD	031.1653/031.1666	SCHOR	2400-05-0012	1

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO 1101-00-0869 PAGE 2 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
27	CABLE CLAMP	832	SMITH	2800-00-0009	1
28	BUSHING NYLINER	4L2FF	THOMN	2800-01-0002	3
29	BUSHING(NYLINER)1/8	2L2FF	THOMN	2800-01-0005	1
30	STANDOFF MALE/FEMALE 1.750 H. .250 HEX 6-32	1473-M03-F03-032	UNICP	2800-02-0010	4
31	STANDOFF. MALE/FEMALE 2.50H. .250 HEX. 4-40	1499-M03-F05-440	UNICP	2800-02-0031	2
32	STANDOFF .500H. .250 HEX. 4-40	2332	SMITH	2800-02-0032	4
33	BAIL ASSY W/FT	180-500	WVTK	2800-08-0010	1
42	SPEEDNUT SELF RETAIN	C7494-632-4	TINN	2800-09-0003	6
34	WASHER. SHOULDER	2668	SMITH	2800-27-0004	22
36	STRAIN RELIEF BUSH	SR6W-1	HEYCO	2800-37-0003	1
R124	POT. TRIM. 200	91AR200	BECK	4600-02-0101	1
50	RES. MF. 1/8W. 1%. 453	RN55D-4530	TRW	4701-03-4530	1
51	RES. MF. 1/8W. 1%. 56.2	RN55D-56R2F	TRW	4701-03-5629	1
37	VARISTOR	V562AB	GE	4799-00-0048	1
38	TRANS	TIP-30	TI	4902-00-0300	1

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO 1101-00-0869 PAGE 3 | REV E

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
39	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1
40	SWITCH ASSY SLIDE	46256-LF	SWCFT	5105-00-0002	1
41	SOLDER GUARD	46256-LF-SG	SWCFT	5105-09-0001	1
43	PWR CORD	0-7789-008-0Y	PACRD	6001-80-0004	1
44	VOLTAGE REGULATOR	MC7815	MOT	7000-78-1500	1

WAVETEK PARTS LIST | TITLE CHASSIS | ASSEMBLY NO 1101-00-0869 PAGE 4 | REV E

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE PARTS LIST CHASSIS

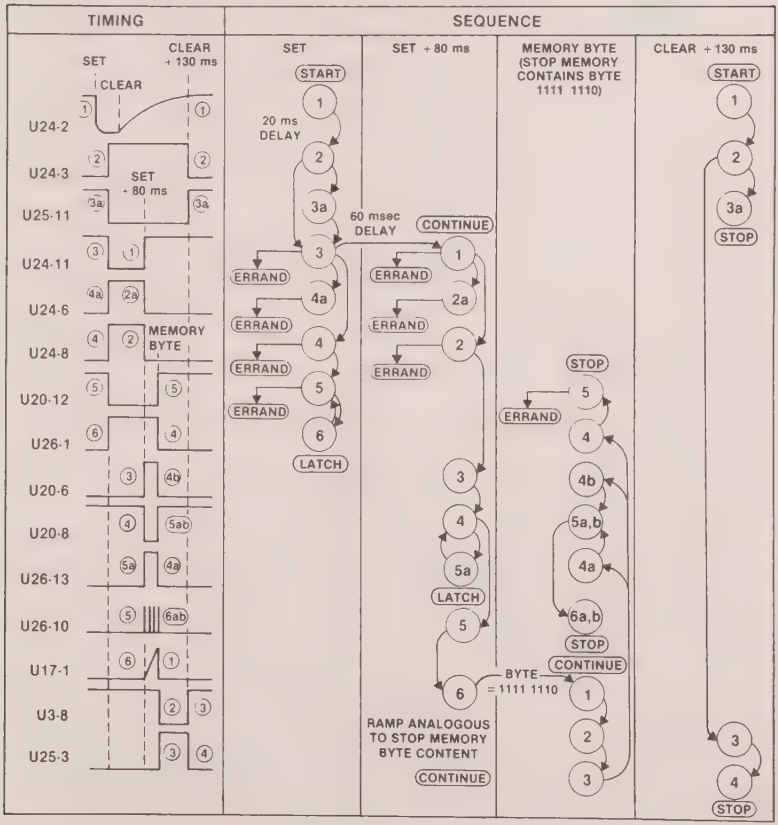
MODEL NO 189 | DRG NO 1101-00-0869 | REV E

TOOL DWG NO 32330 | SHEET | OF 1

APPENDIX A
SET FULL SWEEP TIMING AND SEQUENCE

FRONT PANEL SETUP:
1. Sweep ON/OFF in.
2. RST button in.
3. All other sweep buttons - out.

NOTES:
1. *SET is the instant that FULL SWP button is pressed. CLEAR is the instant that FULL SWP button is released.*
2. *Refer to sequence explanation for full details.*
3. *Although some duplication results, outputs of all gates involved are shown in order to demonstrate sequence.*



SEQUENCE EXPLANATION
SET

1 Front panel FULL SWP button is pressed.

2 After a non-critical time delay of approximately 20 msec due to the time constant of C24, R62, U24-3 goes high.

3a The high from U24-3 applied to U25-12 results in U25-11 going low. Results of this transition, applied to delaying network R60, R61, C23 will be discussed in **1** of "SET +80 msec".

3 The high from U24-3 applied to U24-12 results in U24-11 going low.

ERRAND This low level, output to stop atten. memory U10-14,15 sets stop atten to ÷1.

4a The low from U24-11 applied to U25-4 results in U25-6 going high.

ERRAND This high level, output to the Start DAC Memory U9-2,12 resets the byte content to 0000 0000. (See Data/Gain Truth Table, Figure 4b.)

4 The low from U24-11 applied to U24-10 results in U24-8 going high.

ERRAND This high level, output to the Stop DAC Memory U2-2,12 resets the byte content to 0000 0000.

5 The high from U24-8 applied to U20-1 results in U20-12 going low.

ERRAND This line, referred to as "SET +4V" stops ramp generation and forces +4 Vdc onto the ramp output at U15-1. This is done to prevent interference from the ramp generator during the subsequent operations.

6 The low from U20-12 applied to U26-2 results in U26-1 going high. This **LATCH** applied to U20-2 latches U20-12 (SET +4V) at a low level until receipt of a high level from U25-3 (described in **3** of "Memory Byte = 1111 1110" sequence).

SET +80 ms

1 The low level from U25-11 is applied to delaying network R60, R61, C23. This network has a time constant of approximately 60 msec, resulting in U24-11, 12, 13 forming a 60 msec one-shot MVB. Thus, after this delay, U24-11 goes high, causing sequence to **CONTINUE**. This delay is provided to insure that START/STOP memories U2/U9/U10 are properly reset.

ERRAND The high from U24-11 applied to U10-14, 15 removes the reset condition from these two J-K flip-flops.

2a The high from U24-11 applied to U25-4 results in U25-6 going low.

ERRAND This low level, applied to U9-2, 12 removes the reset condition from this up-counter.

2 The high from U24-11 applied to U2-2, 12 removes the reset condition from this up-counter.

3 The low from U24-8 applied to U20-4 results in U20-6 going high.

4 The low from U24-8 applied to 20-4 results in U20-6 going high.

5a The low from U20-8 applied to U26-11 results in U26-13 going high. Applied to U20-10, this causes U20-8 to **LATCH** at a low level, until receipt of a high from U25-3 (described in **3** of "Memory Byte = 1111 1110" seq).

5 The low from U20-8 applied to U26-9 enables the STOP CLOCK OSCILLATOR U26-4 through 10. Clock pulses at U26-10 increment the STOP MEMORY byte value.

6 The ramp waveform observable at U17-1 is the analog output of U1 STOP DAC as the byte value is incremented from 0000 0000 to 1111 1110.

STOP MEMORY CONTAINS BYTE 1111 1110

1 Stop Memory U2 contains byte = 1111 1110.

2 U3-8 goes low.

3 The low from U3-8 applied to U25-1 (delayed slightly by R59, C22) results in U25-3 going high.

4 The high from U25-3 applied to U26-3 results in U26-1 going low.

4a The high from U25-3 applied to U26-12 results in U26-13 going low.

4b The high from U25-3 applied to U20-5 results in U20-6 going low.

5 The low from U26-1 applied to U20-2 results in U20-12 going high at the next low clock oscillation (U20-11).

ERRAND This high output (SET +4V) removes the +4 Vdc from the ramp generator and allows ramp generation to resume (if no other restrictions such as HOLD, RST, etc are present).

5a,b The low levels from U26-13 and U20-6, ANDED with the next low clock applied to U20-9, 10,11 result in a high at U20-8.

6a,b The high at U20-8 applied to U26-9 disables the STOP CLOCK resulting in cessation of output pulses to the STOP DAC MEMORY U2. Thus, the byte content of 1111 1110 is retained. When applied to the STOP DAC this results in the DATA GAIN-CONTROLLED AMPLIFIER (STOP DAC) having nearly maximum gain.

CLEAR +130 msec

1 When the front panel FULL SWP button is released C24 begins charging through R63 to a high level. The time constant results in a 130 msec delay. This provides a minimum time for all previously described action to occur, even if the button is operated very quickly. The following operations are all HOUSE CLEANING in nature and have no outputs into the memory or ramp circuits.

2 After the 130 msec delay U24-3 goes low.

3a The low from U24-3 applied to U25-12 results in U25-11 going high.

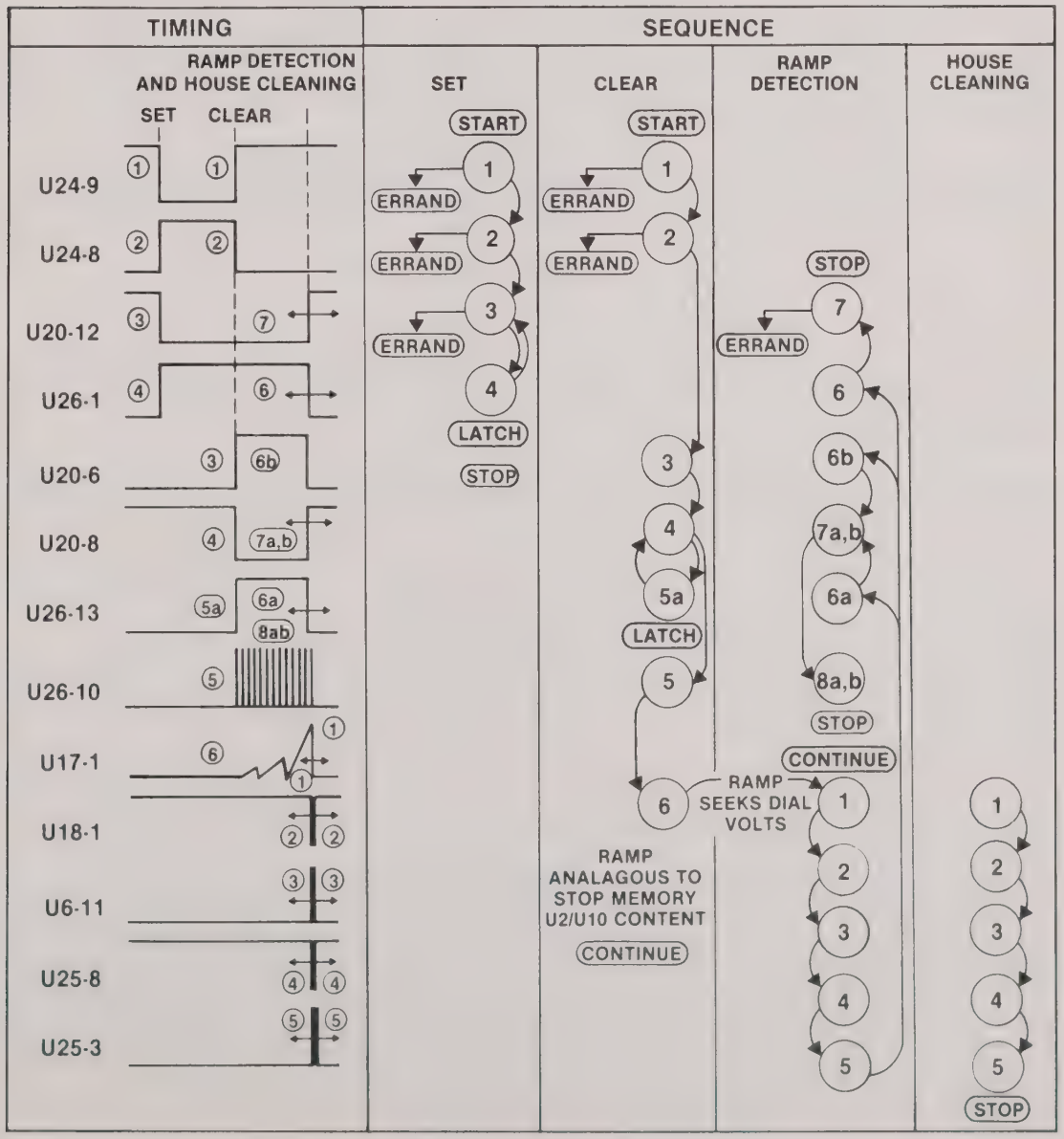
3 The low from U24-3 applied to U3-12 results in U3-8 going high.

4 The high from U3-8 applied to U25-1 results in U25-3 going low.

APPENDIX B
SET STOP TIMING AND SEQUENCE

FRONT PANEL SETUP:
1. Sweep ON/OFF in.
2. RST button in.
3. All other sweep buttons - out.

NOTES:
1. *SET is the instant that SET STOP button is pressed. CLEAR is the instant that SET STOP button is released.*
2. *Refer to sequence explanation for full details.*
3. *Although some duplication results, outputs of all gates involved are shown in order to demonstrate sequence.*
4. *Symbol ↔ indicates edge timing varies with frequency dial setting.*



SEQUENCE EXPLANATION
SET

1 Front panel SET STOP button is pressed.

ERRAND The resulting low level applied to U10-4, 10 sets attenuation memory U10-5, 9 high.

2 The low at U24-9 results in a high at U24-8.

ERRAND This high level output to the stop DAC memory U2-2, 12 resets the byte content to 0000 0000.

3 The high at U24-8 applied to U20-1 results in U20-12 going low.

ERRAND This line, referred to as "SET + 4V" stop ramp generation and forces + 4 Vdc onto the ramp output at U15-1. This is done to provide the stop DAC reference input with a continuous level equal to the maximum ramp amplitude that occurs during normal ramp generation.

4 The low at U20-12 applied to U26-2 results in U26-1 going high. Applied to U20-2, this causes U20-12 to **LATCH** at a low level until receipt of a high from U25-3 (described in **5** of ramp detection sequence).

CLEAR

1 Front panel SET STOP button is released.

ERRAND The resulting high level applied to U10-4, 10 releases the flip flop from set.

2 The high at U24-9 results in U24-8 going low.

ERRAND This low level, applied to U2-2, 12 removes the reset condition, allowing it to count up upon receipt of clock pulses (described in **5** below).

3 The low from U24-8 applied to U20-4 results in U20-6 going high.

4 The high from U20-6 applied to U20-9 results in U20-8 going low.

5a The low from U20-8 applied to U26-11 results in U26-13 going high. This high level, applied to U20-10, causes U20-8 to **LATCH** at a low level until receipt of a high from U25-3 (described in **5** of the ramp detection sequence).

5 The low from U20-8 applied to U26-9 enables the STOP CLOCK OSCILLATOR U26-4 through 10. Clock pulses at U26-10 increment the STOP MEMORY.

6 As the stop memory increments from byte value 0000 0000 to 1111 1111, a ramp waveform will result at U17-1. The stop memory may have to count through all values. As many as 3 times before this operation is halted. The first time through the count, the input reference to U1-14 is attenuated by 100 by the DATA CONTROLLED ATTENUATOR Q10 and Q11. This results in a low-amplitude (0 - 0.04 Vdc) ramp being generated at U17-1. If no match is found between U17-1 and the DIAL VOLTS present at U18-3, the DATA CONTROLLED ATTENUATOR is set to attenuate the DAC input reference by 10. (Low at U2-6 applied to U10-1,13 results in U10-9 going low-turning off Q11). The second time through the count results in a medium-amplitude (0-0.4V) ramp being generated at U17-1. If no match is found in this range, a second low at U2-6 applied at U10-1,13 results in U10-5 going low, turning off Q10. This sets the DATA CONTROLLED ATTENUATOR to

unity gain. The third time the stop memory U2 counts through its range the resulting ramp at U17-1 is 0 to > + 4 Vdc. If all circuits are functional and properly calibrated, there will be a time when the ramp at U17-1 will equal the DIAL VOLTS setting.

RAMP DETECTION

1 The voltage at U17-1 equals the DIAL VOLTS setting. Note that DIAL VOLTS is controlled by the front panel frequency dial. The height and number of ramps at U17-1, as well as the time of occurance of all transitions in this section depend on this setting.

2 When U18-2 > U18-3, then U18-1 goes low.

3 The low from U18-1 applied to U7-12 results in U6-11 going high.

4 The high from U6-11 applied to U25-9 results in U25-8 going low.

5 The low from U25-8 applied to U25-2 results in U25-3 going high.

6 The high from U25-3 applied to U26-3 results in U26-1 going low.

6a The high from U25-3 applied to U26-12 results in U26-13 going low.

6b The high from U25-3 applied to U20-5 results in U20-6 going low.

7 The low from U26-1 applied to U20-2 results in U20-12 going high on the next low clock at U20-11.

ERRAND "SET + 4V" goes high, removing this forcing condition on the ramp generator. This signals the end of SET STOP operation and allows normal ramp generation to resume.

7a,b The low levels from U26-13 and U20-6, ANDED with the next low clock applied to U20-9, 10, 11 result in a high at U20-8.

8a,b The high at U20-8 applied to U26-9 disables the STOP CLOCK resulting in the proper byte value stored in U2.

HOUSE CLEANING

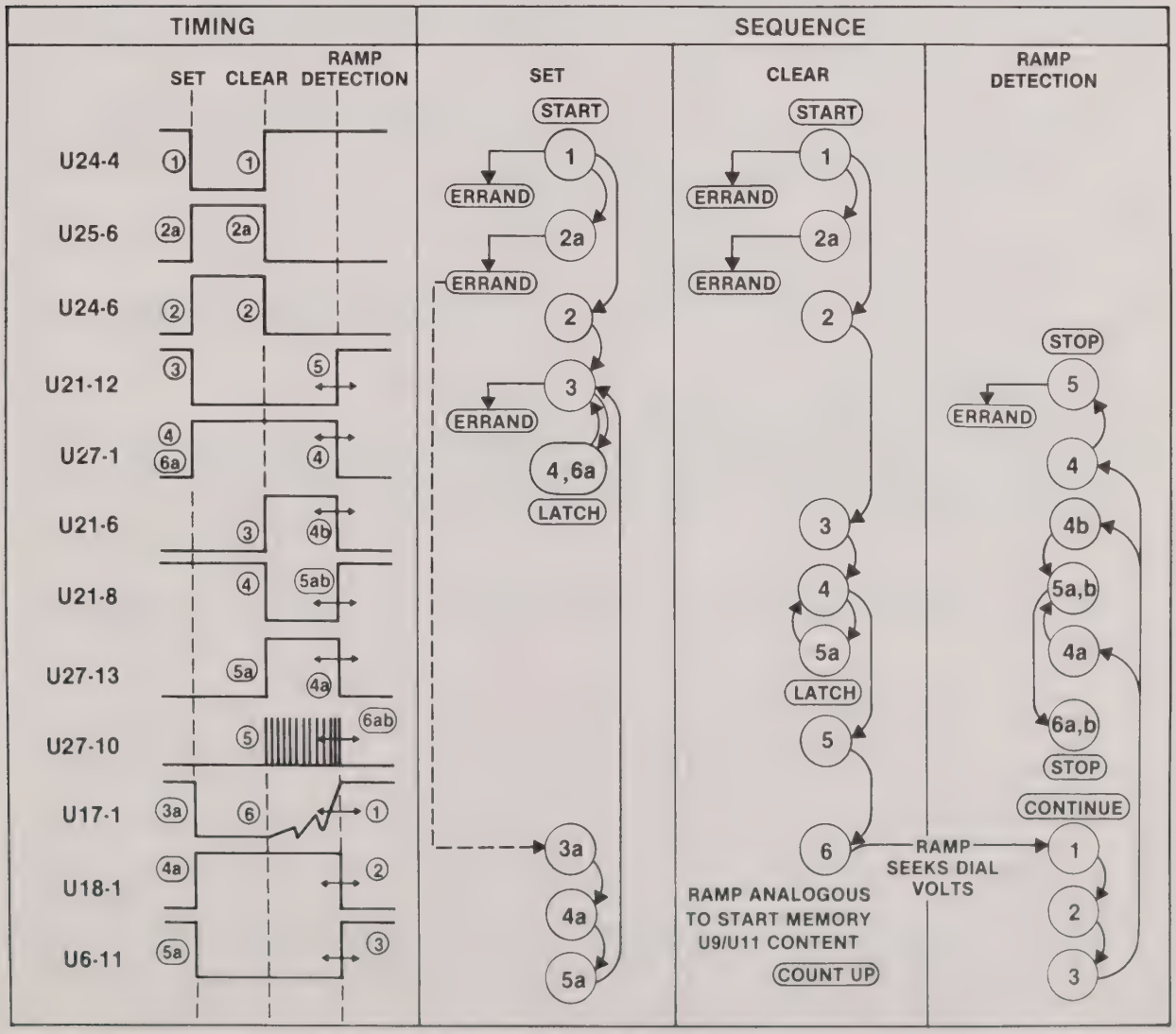
The following operations are HOUSE CLEANING in nature and have no outputs into the memory or ramp circuits.

1. Since U17-1 is in reset mode, the ramp is forced to 0 volts.
2. The low from U17-1 causes U18-1 to go high.
3. The high from U18-1 causes U6-11 to go low.
4. The low from U6-11 causes U25-8 to go high.
5. U25-8 causes U25-3 to go low.

APPENDIX C
SET START TIMING AND SEQUENCE

FRONT PANEL SETUP:
1. Sweep ON/OFF in.
2. RST button in.
3. All other sweep buttons - out.

NOTES:
1. *SET is the instant that SET START button is pressed. CLEAR is the instant that SET START button is released.*
2. *Refer to sequence explanation for full details.*
3. *Although some duplication results, outputs of all gates involved are shown in order to demonstrate sequence.*
4. *Symbol ↔ indicates edge timing varies with frequency dial setting.*



APPENDIX C (CONT)

SEQUENCE EXPLANATION
SET

1 Front panel SET START button is pressed.

ERRAND The resulting low level applied to U11-4, 10 sets U11-5, 9 high.

2 The low at U24-4 results in a high at U24-6.

2a The low at 25-5 results in a high at U25-6.

ERRAND The resulting high level, applied to U9-2, 12 resets the start DAC memory byte content to 0000 0000.

3 The high at U24-6 applied to U21-1 results in U21-12 going low.

ERRAND This line, referred to as SET 0V stops ramp generation and forces 0V onto the ramp output at U15-1. This is done to provide the start DAC reference input with a continuous level equal to the minimum ramp amplitude that occurs during normal ramp generation.

3a As a result of the **ERRAND** signals sent out in **2a** and **3** above (Ramp = 0V and Start DAC Memory = 0000 0000). The voltage at U17-1 drops to zero.

4a The low level from U17-1, compared with the dial volts at U18-2, 3 (assuming the frequency dial is set at 4.0) results in U18-1 going high.

5a The high from U18-1 applied to U6-12 results in U6-11 going low.

4,6a The low from U21-12 ANDED with the low from U6-11 applied to U27-2, 3 results in U27-1 going high. This high applied to U21-2 causes U21-12 to **LATCH** until receipt of a high from U6-11 (described in **3** of the ramp detection sequence).

CLEAR

1 Front panel SET START button is released.

ERRAND The resulting high level applied to U11-4, 10 releases the Flip-Flop from the SET condition.

2 The high at U24-4 results in a low at U24-6.

2a The high at U25-5 results in a low at U25-6.

ERRAND This low level, applied to U9-2, 12 removes the reset condition, allowing U9 to count up upon receipt of clock pulses (described in **5** below).

3 The low from U24-6 applied to U21-4 results in a high at U21-6.

4 The high from U21-6 applied to U21-9 results in a low at U21-8.

5a The low at U21-8 applied to U27-11 results in a high at U27-13. This high level, applied to U21-10, causes U21-8 to **LATCH** at a low level until receipt of a high from U6-11 (described in **3** of the ramp detection sequence).

5 The low from U21-8 applied to U27-9 enables the START CLOCK OSCILLATOR U27-4 through 10. Clock pulses at U27-10 increment the START MEMORY U9.

6 As the START MEMORY increments, the action that results is similiar to that described in **6** of the SET STOP clear sequence explanation, substituting START IC numbers for the STOP numbers referenced.

RAMP DETECTION

1 The voltage at U17-1 equals the DIAL VOLTS setting. Note that DIAL VOLTS is controlled by the front panel frequency dial. The height and number of ramps at U17-1, as well as the time of occurance of all transitions in this section depend on this setting.

2 When U18-2 > U18-3, then U18-1 goes low.

3 The low from U18-1 applied to U6-12 results in U6-11 going high.

4 The high from U6-11 applied to U27-3 results in U27-1 going low.

4a The high from U6-11 applied to U27-12 results in U27-13 going low.

4b The high from U6-11 applied to U21-5 results in U21-6 going low.

5 The low from U27-1 applied to U21-2 results in U21-12 going high at the next low clock from U27-10.

ERRAND SET 0V goes high, removing this forcing condition on the ramp generator. This signals the end of SET START operation and allows normal ramp generation to resume.

5a,b The low levels from U27-13 and U21-6 ANDED with the next low clock applied to U21-9, 10, 11 result in U21-8 going high.

6a,b The high from U21-8 applied to U27-9 disables the START CLOCK resulting in the proper byte value being stored in U9.

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